DESIGNING HARMONIC FILTERS FOR ADJUSTABLE SPEED DRIVES TO COMPLY WITH NEW IEEE-519 HARMONIC LIMITS

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Abstract - This paper discuses the application of the revised IEEE-519 Harmonics standards to typical industrial facilities employing adjustable speed drives (ASDs). The harmonic generation characteristics of ASDs are described. Requirements for control of the harmonic currents are developed as a function of the ASD characteristics, overall plant loading level, power system characteristics, and power factor correction requirements. Filter design procedures are presented for controlling the harmonic currents injected onto the power system.

INTRODUCTION

The increasing application of power electronic equipment (especially adjustable speed motor drives, or ASDs) in the industrial environment has led to a growing concern for harmonic distortion and the resulting impacts on system equipment and operations. Possible problems include transformer overheating, motor failures, fuse blowing, capacitor failures, and misoperation of controls. [1]

Harmonic currents are generated by the operation of nonlinear loads and equipment on the power system. These include ASDs, other power converter equipment, voltage controllers, transformers, and arcing loads. Voltage distortion results from the interaction of these currents with the system impedance vs. frequency characteristics.

A revised version of IEEE Standard 519, "Recommended Practice for Harmonic Control in Electric Power Systems", provides recommended limits for harmonics in two categories [2]:

1. Harmonic current limits are specified for individual customers. These are evaluated at the point of common coupling between the customer and the power system.

2. Harmonic voltage limits are specified for the overall power system and provide an indication of the power quality that a customer can expect.

This paper discusses these limits and their application to typical industrial facilities employing ASDs. The harmonic generation characteristics of ASDs are developed and then the expected harmonic levels are evaluated for different power system characteristics and power factor correction practices. Finally, filter design procedures are developed for controlling the harmonic currents.

ASD CHARACTERISTICS

The characteristics of the input current for ASDs depend on the drive type, drive loading, and the characteristics of the system supplying the drive. The harmonic distortion in these currents can vary over a wide range. However, it is possible to identify two basic waveform types that can be used for analysis purposes:

TYPE 1: High Distortion Current Waveform
This is characteristic of virtually all ASDs that have voltage source inverters (either stepped wave or pulse width modulated) that do not have additional choke inductance for current smoothing. The total harmonic distortion for the selected waveform is 80%. Actually, it can be higher for small drives but this waveform is a good representation for larger drives or groups of smaller drives.

TYPE 2: Normal Distortion Current Waveform
This waveform represents dc drives, large ac drives with current source inverters, and smaller ac drives with voltage source inverters and added inductance for current smoothing. The selected waveform has a distortion level of 38%, which is obtained from a 100 hp PWM drive with a 3% choke inductor. DC drives and larger ac drives could have somewhat lower distortion levels (e.g. 25-30%).

Example waveforms and harmonic spectrums for the two waveform types are given in Figure 1. These waveform characteristics are used throughout the paper to evaluate harmonic control requirements.

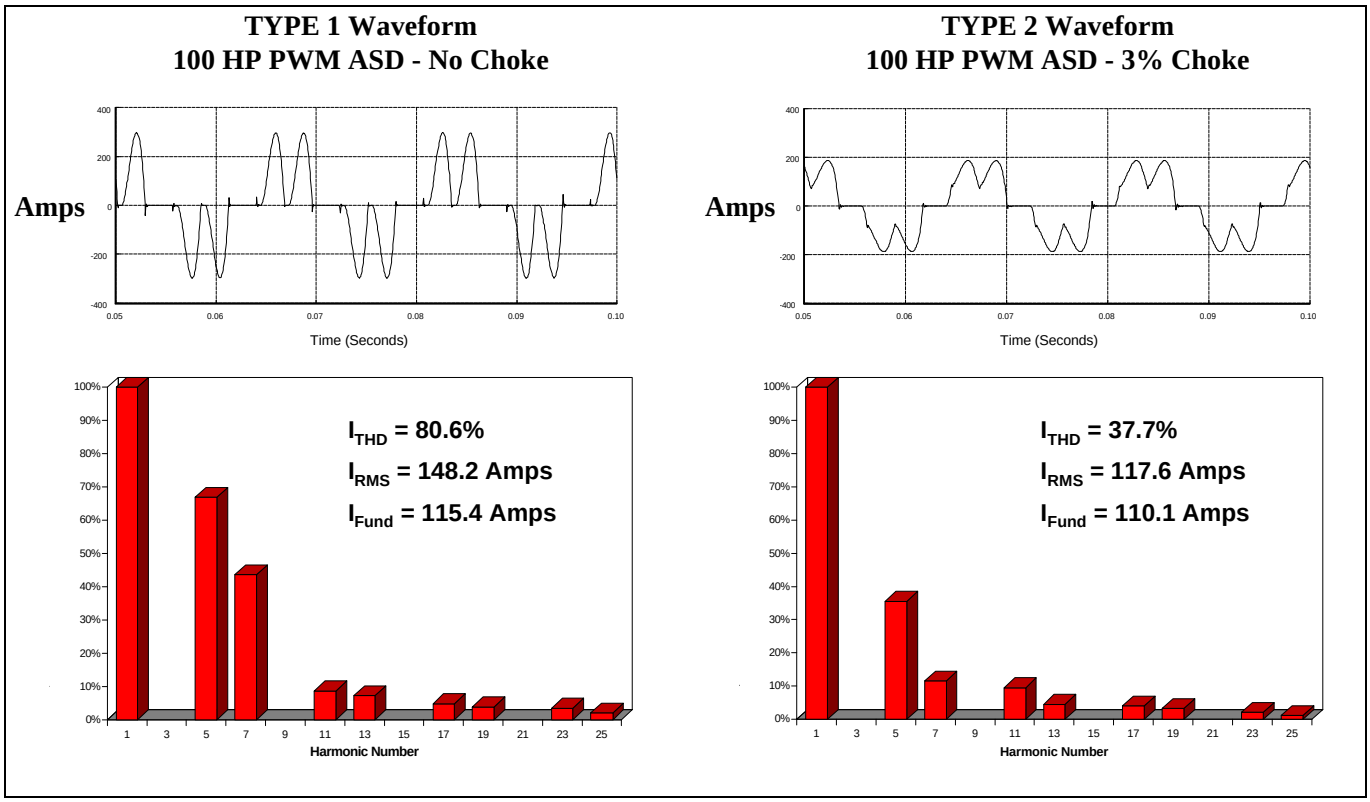


Figure 1. Example ASD Current Waveforms Used for Analysis

The first observation from these two waveform types is the significant harmonic reduction that can be obtained for PWM type ASDs just by adding a choke inductance at the input. Figure 2 illustrates the effect of choke inductor size on input current distortion levels for a typical drive. [3] Some drive manufacturers are starting to include this choke inductance in the dc link of the drive, providing the same harmonic current reduction benefit.

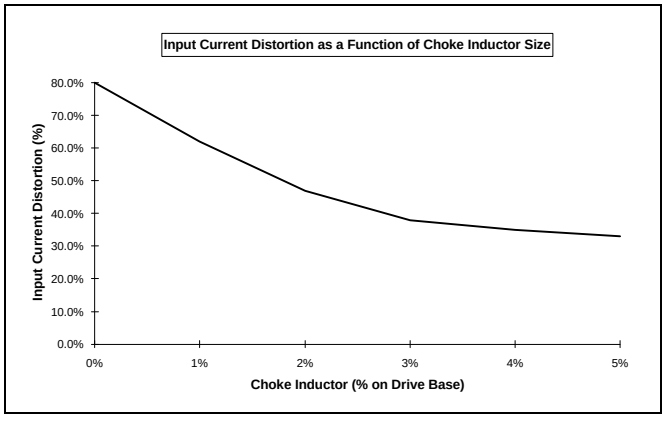


Figure 2. Effect of Input Choke on ASD Current Distortion

IEEE-519 HARMONIC CURRENT LIMITS

The revised version of IEEE-519 defines harmonic current limits for individual customers (Table 1). These are designed to limit the injection of harmonic currents onto the power system so that the resulting voltage distortion will be acceptable for all customers.

Table 1
IEEE 519 Harmonic Current Limits.

Maximum Harmonic Current Distortion in % of Maximum Load Current

Harmonic Order (odd harmonics)

I_{SC}/I_L	<11	11≤h<17	17≤h<23	23≤h<35	35≤	TDD
<20	4.0	2.0	1.5	0.6	0.3	5.0
20-50	7.0	3.5	2.5	1.0	0.5	8.0
50-100	10.0	4.5	4.0	1.5	0.7	12.0
100-1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

Where: I_{SC} = Maximum short circuit current at PCC
I_L = Maximum demand current (60 Hz) at PCC
TDD = Total Demand Distortion

Table 10.2
IEEE 519 - Draft

In order to evaluate a facility with respect to these harmonic current limits, a few terms need to be defined.

Point of Common Coupling (PCC) - this is the location where the harmonic currents are evaluated. It will probably be determined by the utility. Likely locations are the metering point or the high side of the customer step down transformer.

Average Maximum Demand Load Current (I_L) - All harmonic current limits in the standard are given in percent of this value. It is defined as the average of the monthly maximum demand values for 12 months. Obviously, this must be estimated for new customers or customers who have made changes to their load.

Short Circuit Ratio (SCR=Isc/I_L) - This is the ratio of the short circuit current at the point of common coupling to the average maximum demand load current, I_L. A strong system with respect to the customer size will result in high values for the SCR. Higher levels of harmonic current generation are allowed for higher values of SCR because a single customer has less impact on the system voltage distortion.

For purposes of analysis in this paper, we will use an example system with a single step down transformer to 480 Volts as shown in Figure 3. The impacts of harmonic generation from adjustable speed drives in this system are evaluated in the following sections. The short circuit ratio assumed puts us in Row 2 of Table 1. These limits will be used for the analysis in the following sections.

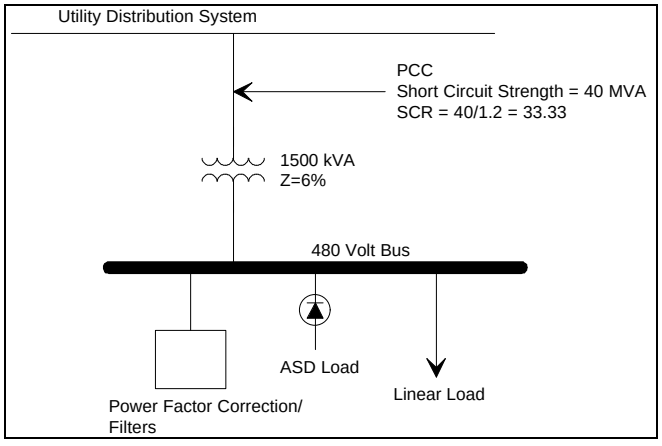


Figure 3. Example System Used for Analysis.
Note: Customer Avg. Max. Demand Load = 1200 kVA

EVALUATING HARMONIC LIMITS WITH NO CAPACITORS OR FILTERS

The simplest system configuration assumes that there are no power factor correction capacitors and no harmonic filters. For this condition, the harmonic currents generated by ASD loads can be assumed to flow through the step down transformer and on to the primary system (i.e. no magnification and no filtering). With this assumption, limits for ASD plant loading can be derived using the current waveforms provided previously.

The ASD plant loading needs to be expressed as a percentage of the average maximum demand load used to evaluate the harmonic limits (1200 kVA in this case). Once this is done, the ASD harmonics can be referred to the 1200 kVA base and compared with the limits in Table 1. The fifth harmonic current component will usually be the limiting factor for this evaluation. Figure 4 gives the fifth harmonic current for the entire plant as a function of the plant ASD loading for the two characteristics waveforms.

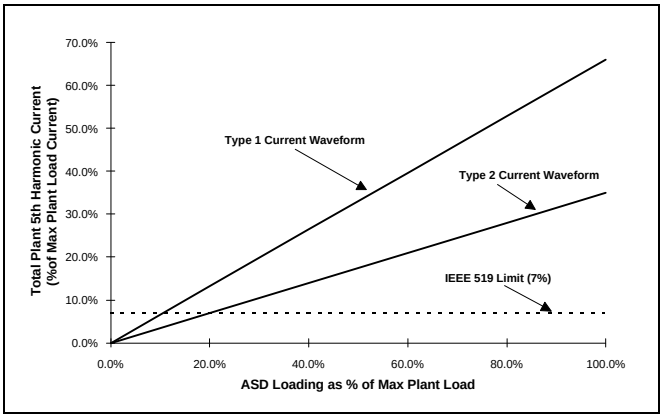


Figure 4. Evaluation of Fifth Harmonic Current as a Function of the Total ASD Plant Load

Figure 4 illustrates that only a small percentage of the plant load can be ASDs for this example facility:

≈ 10% for TYPE 1 currents
≈ 20% for TYPE 2 currents

An assumption inherent in this simple evaluation is that the harmonics from multiple ASDs add directly. This is approximately true for the lower order harmonic components from PWM-type ASDs. It is not at all true for dc drives where cancellation of 50% or more is common. This means that dc drives could be over 40% of the plant load without exceeding IEEE-519 limits.

EVALUATING HARMONIC LIMITS WITH POWER FACTOR CORRECTION CAPACITORS

The addition of power factor correction capacitors at the 480 Volt level causes a parallel resonance between the capacitors and the system source inductance (Figure 5). Harmonic current components that are close to the parallel resonant frequency are magnified. Higher order harmonic currents at the point of common coupling are reduced because the capacitors are a low impedance at these frequencies.

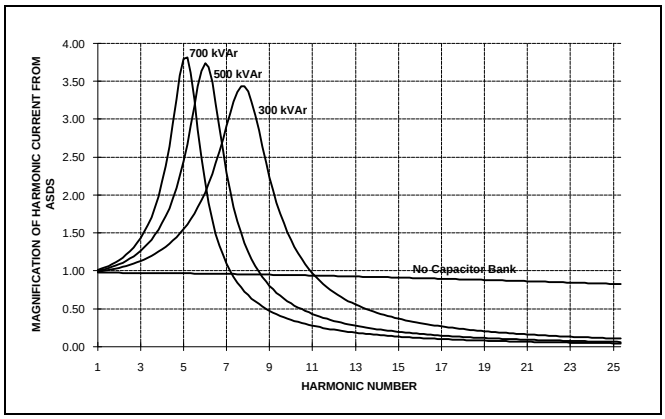


Figure 5. Effect of Capacitor Additions on the Harmonic Current at the PCC

Figure 5 illustrates that typical sizes of power factor correction capacitors will result in magnification of the fifth and seventh harmonic components from the ASDs. This makes it even more difficult to meet the IEEE-519 harmonic current limits. Basically, power factor correction capacitors should not be used without tuning reactors if ASDs are a significant percentage of plant load (e.g. > 10%).

HARMONIC CONTROL WITH TUNED CAPACITOR BANKS

The simplest method to provide some level of harmonic control and also accomplish power factor correction requirements is to add the power factor correction in the form of tuned capacitor banks. This prevents magnification of any characteristic harmonic components from the drives. The capacitor/reactor configuration is shown in Figure 6.

The tuned frequency for the serious reactor/capacitor combination is selected somewhere below the fifth harmonic (e.g. 4.7) to prevent a parallel resonance at any characteristic harmonic. Figure 7 illustrates the effect of the tuned bank on the harmonic currents at the point of common coupling. Significant reduction of the fifth harmonic from the ASDs is obtained and there is some reduction at all the harmonic components (i.e. no magnification).

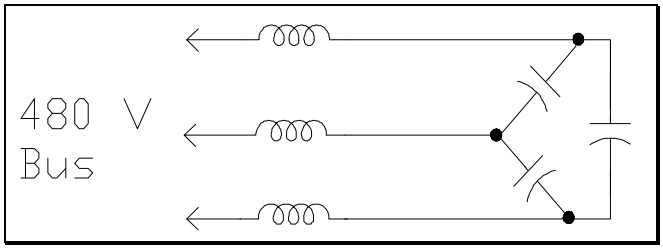


Figure 6. Basic Configuration for a Tuned Capacitor Bank for Power Factor Correction and Harmonic Control

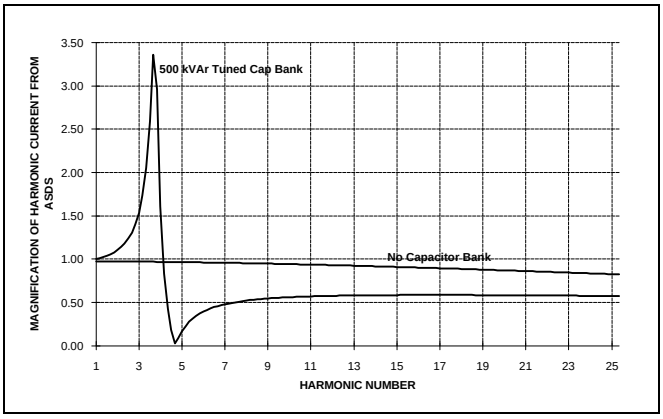


Figure 7. Effect of Tuned Capacitor Bank on the Harmonic Current at the PCC

With the tuned capacitor bank, the seventh or the eleventh harmonic component from the ASDs will be the limiting component when evaluating the IEEE-519 limits. Figure 8 plots both of these harmonic components at the PCC as a function of the plant ASD loading with a 500 kVAr tuned bank (tuned to 4.7 as illustrated in Figure 7). Figure 8a shows that the seventh harmonic is the limiting case for a TYPE 1 current waveform. The ASD loading should be limited to about 35% of the maximum plant load in this case.

The eleventh harmonic is the limiting case for a TYPE 2 current waveform when a tuned bank is used to control the lower order harmonics. Figure 8b shows that approximately 60% of the maximum plant load can be ASDs in this case. Actually, the ASD loading could even be somewhat higher than this if there are multiple ASDs because some cancellation should be expected at these higher harmonic frequencies.

Design of the 4.7th tuned bank must take into account the maximum harmonic generation levels in the plant and also

the harmonics which may be absorbed from the higher voltage power system. It is a good conservative practice to assume that all the fifth harmonic from the ASDs will flow in the tuned bank and then estimate the contribution from the system using a measurement (or estimate) of the system 5th harmonic voltage distortion. The spreadsheet in Appendix A provides a breakdown of the required filter component ratings for this example case (60% of plant load is ASDs with TYPE 2 input current waveform).

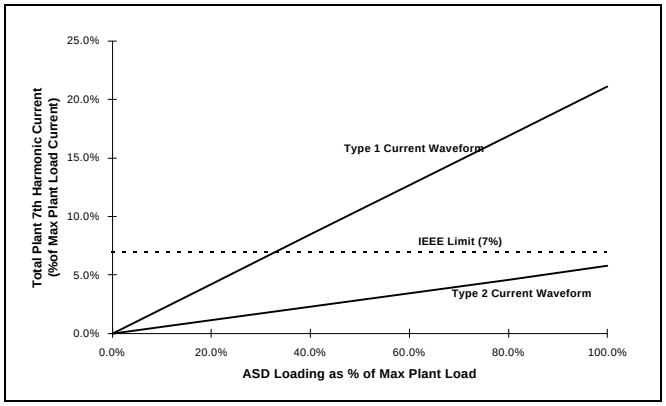


Figure 8a. Seventh harmonic component of the plant load current as a function of ASD loading with a 4.7 tuned bank.

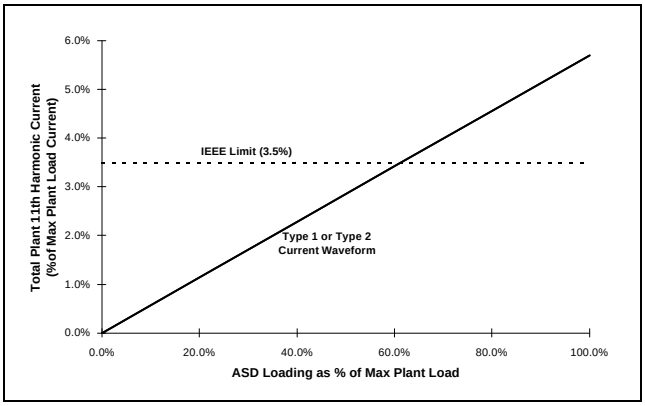


Figure 8b. Eleventh harmonic component of the plant load current as a function of ASD loading with a 4.7 tuned bank.

GENERAL FILTER DESIGN PROCEDURE

In special cases where a combination of input chokes for the ASDs and tuned capacitor banks are not sufficient to control harmonic current levels, a more complicated filter design may be required. Individual tuned steps will be needed to control the individual harmonic components of concern. This is often difficult and a more detailed harmonic study will normally be required. Figure 10 gives the general procedure for designing these filters.

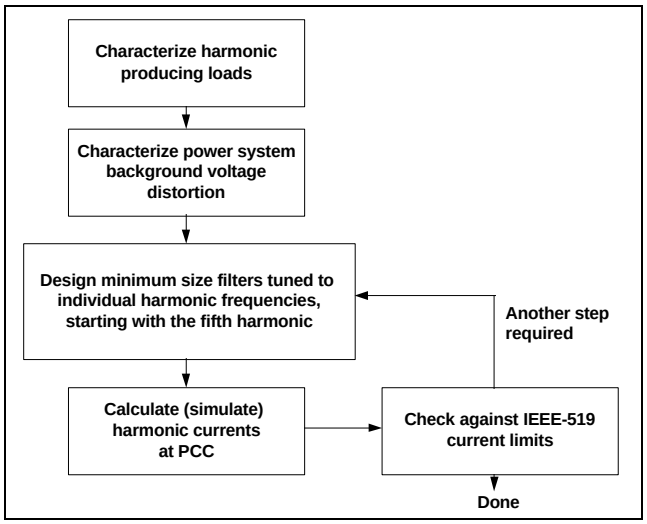


Figure 10. General procedure for designing individually tuned filter steps for harmonic control.

There are a few important problems with this approach:

1. Significant derating of the filters may be required to handle harmonics from the power system. Including the contribution from the power system is part of the process of selecting a minimum size filter at each tuned frequency - they must be large enough to absorb the power system harmonics.

2. The design may result in excessive kVAr due to the number of filter steps and filter sizes needed for harmonic control. This would result in leading power factor and possible overvoltages.

3. In some rare cases, even three or four steps (5,7,11 or 5,7,11,13) may not be sufficient to control the higher order harmonic components to the levels specified in IEEE 519.

If these problems result in unacceptable filter designs, it may be possible to control the harmonics with different types of drives (e.g. 12 pulse or 18 pulse configurations) or electronically with active filters.

CONCLUSIONS/SUMMARY

The following summarizes important results of the analysis presented in this paper. The conclusions in Table 2 apply primarily to PWM type ASDs (these are the most common). Dc drives and other types of ac drives are likely to have greater cancellation of harmonics from multiple drives and the results summarized here can be considered very conservative for these drive types.

Table 2
Rules of Thumb for Maximum ASD Plant Loading
(% of Maximum Plant Load)

Condition	TYPE 1 Characteristic (No Choke)	TYPE 2 Characteristic (3% Choke)
Simple System - No Caps, No Filters	10%	20%
480 Volt PF Correction Caps	<10% (Must be Analyzed)	<20%
480 Volt Tuned Caps to 4.7th Harmonic	35%	60%
480 Volt Filters - Multiple Steps	>35% (Must be Analyzed)	>60%

REFERENCES

[1] D.E. Rice, "Adjustable Speed Drive and Power Rectifier Harmonics - Their Effect on Power System Components," IEEE IAS Transactions, 1984.

[2] Revised Standard IEEE 519, "Recommended Practices and Requirements for Harmonic Control in Power Systems," Approval June, 1992.

[3] T.E. Grebe, M.F. McGranaghan, and M. Samotyj, "Solving Harmonic Problems in Industrial Plants and Harmonic Mitigation Techniques for Adjustable Speed Drives," Electrotech 92 Proceedings, Montreal, June 14-18, 1992.

Appendix A. Example Design Calculations for 4.7th Tuned Bank

Low Voltage Filter Calculations:

SYSTEM INFORMATION:

Filter Specification:	5 th	Power System Frequency:	60 Hz
Capacitor Bank Rating:	500 kVAr	Capacitor Rating:	480 Volts 60 Hz
Nominal Bus Voltage:	480 Volts	Derated Capacitor:	500 kVAr
Capacitor Rated Current:	601.4 Amps	Total Harmonic Load:	750 kVA
Filter Tuning Harmonic:	4.7 th	Filter Tuning Frequency:	282 Hz
Cap Impedance (wye equivalent):	0.4608 W	Cap Value (wye equivalent):	5756.5 uF
Reactor Impedance:	0.0209 W	Reactor Rating:	0.0553 mH
Filter Full Load Current:	629.9 Amps	Supplied Compensation:	524 kVAr
Transformer Nameplate: *(Rating and Impedance)*	1500 kVA 6.00 %	Utility Side Vh: *(Utility Harmonic Voltage Source)*	2.50 % THD
Load Harmonic Current:	33.33 % Fund	Load Harmonic Current:	300.7 Amps
Utility Harmonic Current:	119.1 Amps	Max Total Harm. Current:	419.8 Amps

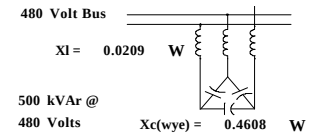
CAPACITOR DUTY CALCULATIONS:

Filter RMS Current:	757.0 Amps	Fundamental Cap Voltage:	502.8 Volts
Harmonic Cap Voltage:	67.0 Volts	Maximum Peak Voltage:	569.8 Volts
RMS Capacitor Voltage:	507.2 Volts	Maximum Peak Current:	1049.7 Amps

CAPACITOR LIMITS: (IEEE Std 18-1980)

	Limit		Actual
Peak Voltage:	120%		119%
Current:	180%		126%
KVAr:	135%		133%
RMS Voltage:	110%		106%

FILTER CONFIGURATION:



FILTER REACTOR DESIGN SPECIFICATIONS:

Reactor Impedance:	0.0209 W	Reactor Rating:	0.0553 mH
Fundamental Current:	629.9 Amps	Harmonic Current:	419.8 Amps