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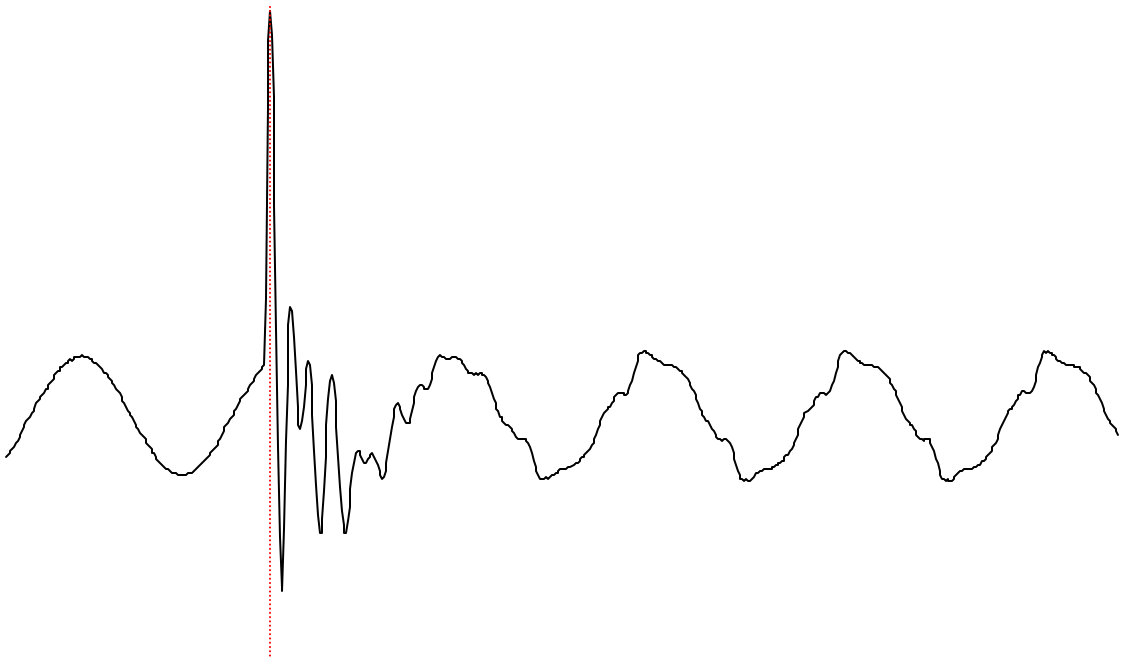
Harmonics and Transients Tech Notes



Issue # 00-2 ***June 2000*** ***Editor: Karen Brown***

Project Manager: Tom Grebe

In this issue:

Letter from the Editor:

Dear PATH Members:

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Sincerely,

Karen Brown
Technical Coordinator
Editor, PATH Users Group / PQView User Group

THE FUNDAMENTALS OF POWER QUALITY

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Abstract: This paper describes the fundamental issues relating to power quality such as power factor and total harmonic distortion. These issues are described in the context of the full wave rectifier circuit with output filter capacitor. This circuit is commonly used as the input stage of a power supply and is a good example of poor power quality. Original equations are derived for peak currents and power factor, from which the total harmonic distortion can be found. The effect of non-linear loads on the neutral current in three-phase operation is discussed.

Introduction

The electronics industry is not immune from the increased awareness of environmental issues. Proliferation of computer equipment and industrial drives causes 'pollution' of the ac mains in the form of unwanted harmonics of the fundamental ac frequency. Switching currents used in power supplies and inverter motor drives generates these harmonics. Harmonics create losses in the electrical supply system and larger transformers are needed to supply these losses. European and American electrical industries are introducing standards to limit unwanted harmonics in order to improve power quality.

The purpose of this paper is to describe the issues involved in power quality analysis in terms of circuits, which are familiar and readily explained to undergraduate students. Traditionally, power factor has been defined in terms of the phase difference between a sinewave of voltage and a sinewave of current. This definition is expanded to include non-sinusoidal waveforms. It turns out that the capacitor filtered full wave rectifier circuit is a very good example of poor power quality. The paper derives useful approximations for all quantities of interest such as voltage ripple, peak input current. The power factor of the circuit is calculated and shown to be very poor.

PSPICE models are presented along with harmonic analysis. Experimental results are also given.

Power Factor

A power converter changes the characteristics of electrical supply from one form at the source to another form at the sink or load. Figure 1 shows a regulated dc power supply where the input ac source is converted to a dc output. A full wave rectifier, with an output filter capacitor, would generate the waveforms shown in Figure 1. The power factor of the source is defined as the ratio of real to apparent power

$$k_p = \frac{\langle p \rangle}{V_s\, I_s} \qquad (1)$$

where <p> is the average power delivered to the circuit and V_s and I_s are the R.M.S. values of the input voltage and current respectively. Over an integral number of cycles of period T

$$\langle p \rangle = \frac{1}{T}\int_0^T v(t)i(t)\,dt$$

The R.M.S. values of v_s and i_s may be calculated from the waveforms, for waveform v(t) the R.M.S. value is V:

$$V = \sqrt{\frac{1}{T}\int_0^T v^2(t)\,dt}$$

Evidently, knowledge of the voltage and current waveforms allows the power factor to be calculated.

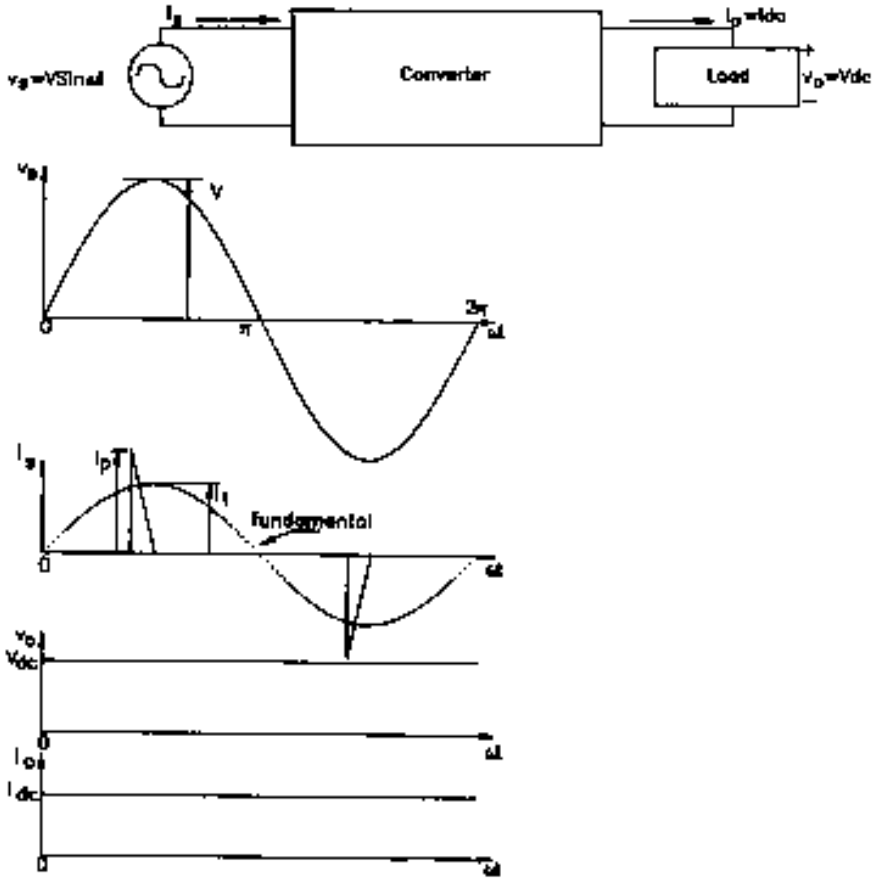

Figure 1: Power Supply and Associated Waveforms

The Fourier Series of a non-sinusoidal waveform is given by:

$$i(t) = I_o + \sum_{n=1}^{\infty} a_n \cos n\omega t + b_n \sin n\omega t$$

$$I_0 = \frac{1}{2\pi}\int_0^{2\pi} i(\omega t)\, d(\omega t)$$

$$a_n = \frac{1}{\pi}\int_0^{2\pi} i(\omega t)\cos n\omega t\, d(\omega t)$$

$$b_n = \frac{1}{\pi}\int_0^{2\pi} i(\omega t)\sin n\omega t\, d(\omega t)$$

These expressions are often simplified by recognizing properties such as odd and even functions. When a function is odd a_n is zero and we can write

$$i(t) = I_0 + \mathbf{I}_1 \text{ Sin } \omega t + \mathbf{I}_2 \text{ Sin } 2\omega t + ...$$

where $\mathbf{I}_1$ is the peak value of the fundamental of i(t), etc., the R.M.S. value is $I_1=\mathbf{I}_1/\sqrt{2}$.

The situation in Figure 1is quite common when the voltage waveform is a pure sinusoid and the current contains harmonics. From the definition of <p> the only component of current which will contribute to average power is the fundamental and

$$\langle p \rangle = V_{r.m.s.} I_{1\,r.m.s.} \cos\theta$$

where θ is the phase difference between the voltage waveform and the fundamental of the current waveform. This may be rewritten

$$\begin{aligned}\langle p \rangle &= V_{r.m.s.} I_{r.m.s.} \frac{I_{1\,r.m.s.}}{I_{r.m.s.}} \cos\theta \\ &= V_{r.m.s.} I_{r.m.s.} k_d\, k_\theta\end{aligned} \qquad (2)$$

By definition (1) the power factor is

$$k_p = k_d\, k_\theta$$

where k_d is called the distortion factor and k_θ is called the displacement factor.

$$k_d = \frac{I_{1\,r.m.s.}}{I_{r.m.s.}}$$
$$k_\theta = \cos\theta$$

Evidently, if the current is pure sinewave, k_d is unity, and the power factor definition reverts to the classical case. In Figure 1, θ is 0° and cos θ is unity. However, as we shall see later, the power factor is less than 0.5, due entirely to the distortion in the current waveform.

The total loss due to all the harmonics in i(t) is

$$P = R(I_1^2 + I_2^2 + I_3^2 + ...) = RI_{r.m.s.}^2$$

The total loss due to the fundamental is

$$P = RI_1^2$$

The ratio of the power in all the harmonics except the fundamental to the power loss due to the fundamental is

$$\frac{RI_{r.m.s.}^2 - RI_1^2}{RI_1^2} = \frac{\sum_{n\neq 1} I_n^2}{I_1^2}$$

The Total Harmonic Distortion is the square root of this quantity

$$THD = \sqrt{\frac{\sum_{n\neq 1} I_n^2}{I_1^2}} = \sqrt{\frac{I_{r.m.s.}^2}{I_1^2} - 1} \qquad (3)$$

where I_n is the R.M.S. value of the n^{th} harmonic of current. We can deduce the distortion factor from (3) as

$$k_d = \sqrt{\frac{1}{1+\mathrm{THD}^2}} \qquad (4)$$

The Full Wave Rectifier

The full wave rectifier circuit shown in Figure 2(a) has a sinusoidal input voltage. The filter capacitor C smooths out the rectified sinewave at the expense of short input current pulses. Assuming ideal diodes, and a resistive load, the output current is given by

$$i_o = C\frac{dv_o}{dt} \qquad (5)$$

For a sufficiently large capacitor the voltage ripple is negligible compared to the peak value of the rectified voltage waveform, **V**, and the average output voltage is

$$V_o = RI_o \approx \mathbf{V} \qquad (6)$$

Ridler [1] and Schade [2] analyzed this circuit in detail. The solution involves a transcendental equation, which can be solved by computer analysis. In order to gain insight into the circuit, an approximate analysis is presented, using the approximate waveforms of Figure 2(b). The approximations are reasonably accurate if $RC > 4T$ and the output voltage ripple $\Delta V/V_o < 10\%$, where T is the period of the ac waveform, and ΔV is the voltage ripple as shown in Figure 2.

The capacitor is charged during the period Δt and, for $\Delta t \ll T/2$, the discharge time is approximately T/2.

The average output current is obtained from (5):

$$I_o = C\frac{\Delta V}{\frac{T}{2}-\Delta t} \approx C\frac{\Delta V}{\frac{T}{2}} \qquad (7)$$

Rearranging (7) yields

$$\Delta V = I_o \frac{T}{2C}\left\{1-\frac{2\Delta t}{T}\right\} \approx \frac{I_o}{2fC} = \frac{V_o}{2fRC} \qquad (8)$$

We can approximate the input diode current as a triangle of height I_p. The amps-seconds of the capacitor over a complete cycle must be zero, otherwise there would be an indefinite build-up of charge. Thus,

$$Q = \int i\,dt = \frac{1}{2} I_p \Delta t = I_o \frac{T}{2} \qquad (9)$$

The charging voltage of the capacitor follows the input sinusoidal waveform and for small arguments:

$$\cos x \cong 1 - \frac{x^2}{2}$$

resulting in (see Figure 2(b))

$$\Delta V = \mathbf{V}(1-\cos\omega t) \approx \frac{1}{2}\mathbf{V}(\omega\Delta t)^2 \qquad (10)$$

where $\omega=2\pi f$ and $f=1/T$, rearranging gives

$$\frac{\Delta t}{T} = \frac{1}{\sqrt{2}\pi}\sqrt{\frac{\Delta V}{\mathbf{V}}} \qquad (11)$$

Substituting (11) into (9) and rearrange to obtain the peak diode current:

$$I_p = \sqrt{2}\pi I_o \sqrt{\frac{\mathbf{V}}{\Delta V}} \qquad (12)$$

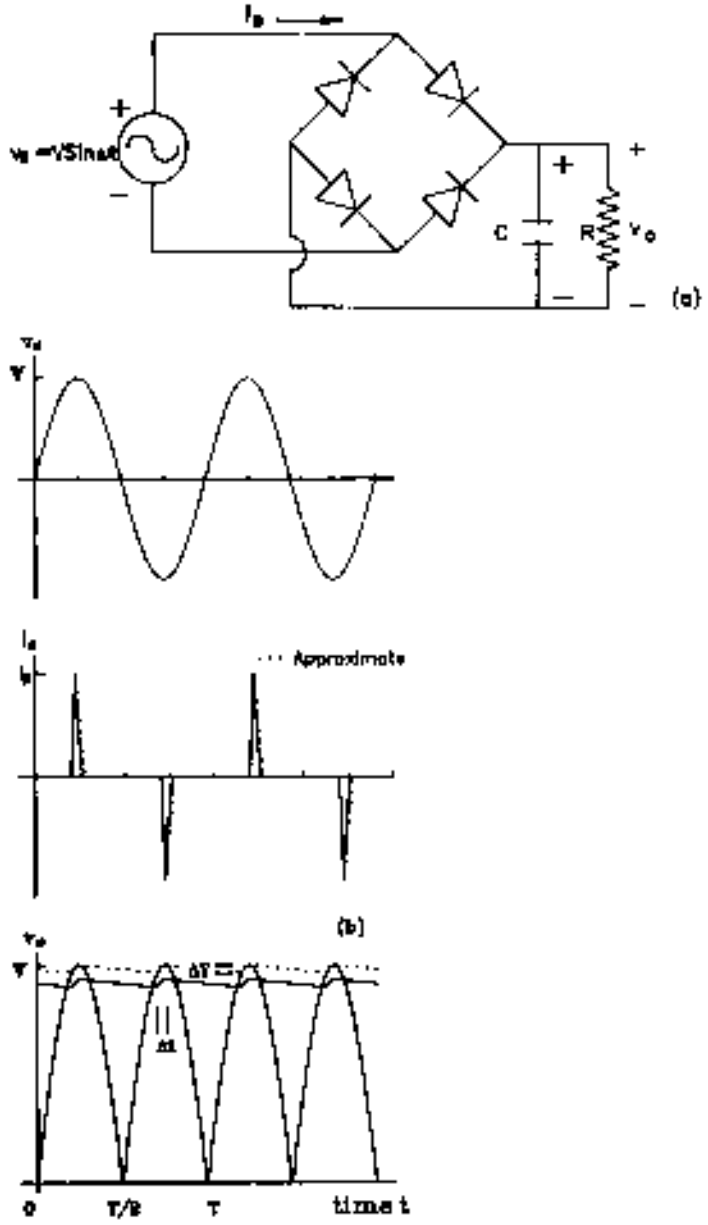

Figure 2: Full Wave Bridge Rectifier (a) Circuit diagram, (b) Input Voltage, Input Current and Output Voltage Waveforms

Power Factor Calculation

With ideal diodes, the average power delivered by the source is equal to the output power

$$\langle p \rangle = V_o I_o = \mathbf{V} I_o$$

The R.M.S. value of the source voltage is

$$V_s = \frac{\mathbf{V}}{\sqrt{2}}$$

The R.M.S. value of the triangular waveform of the source current is

$$I_s = I_p \sqrt{3 \frac{\Delta t}{\frac{T}{2}}}$$

Substituting for I_p from (12) and $\Delta t/T$ from (11) produces an expression for the source current in terms of the output voltage ripple

$$I_s = \frac{2}{\sqrt[4]{2}} \sqrt{\frac{\pi}{3}} I_o \sqrt[4]{\frac{\mathbf{V}}{\Delta V}}$$

Substituting these expressions in the definition of power factor (1) yields a simple expression for k_p

$$k_p = \frac{\langle p \rangle}{V_s I_s} = 0.82 \sqrt[4]{\frac{\Delta V}{\mathbf{V}}} = 0.75 \sqrt[4]{\frac{\Delta V}{V_s}} \qquad (13)$$

This simple expression clearly shows that reducing the output ripple also reduces the input power factor, what is surprising is that it has a fourth root dependence. For instance, halving ΔV reduces k_p by about 15%. For ΔV=10% of V_s, k_p=0.42.

The result in (13) may be obtained from the definition of the distortion factor, k_d, in section II, since k_θ=1.

Experimental Results: Full Wave Bridge Rectifier

A full wave bridge rectifier with a capacitor filter was constructed with the following circuit parameters:

V_s = 17.7 V R.M.S. at 50 Hz, **V**=25 V
R = 22
C = 10,000μF

In a practical circuit there is always some source resistance in addition to the resistance of the conducting diodes. This source resistance is very critical to the input current and power factor calculations. It is relatively straightforward to include this in our analysis. The analysis with R_s do not shed any further light on the concepts developed so far, however for clarity the details are given in Appendix A; In the following results section both cases are calculated, i.e. R_s=0 and R_s=0.33 . The calculations are compared with results from a PSPICE simulation and finally experimental results are given. The results are summarized in Table 1. The average output voltage is calculated using (6), with a further 1.5 V subtracted to account for two diode drops. With Rs=0.33 , (A4) is iterated to obtain V_0 and I_0. The voltage ripple is calculated using (8). The peak diode current is calculated from (12) and (A5) and finally (13) and (A7) yield the power factor. The Total Harmonic Distortion is found from (4), assuming k_θ=1 and k_d=k_p. There is a very small displacement angle, which can be seen by examining Figure 2(b). The capacitor charging process is not centered exactly on the peak of the input voltage waveform. Applying (4) to the experimental results would suggest k_d=0.637 and k_θ=0.989 or θ=8.5 for k_p=0.63. Examination of the results shows that varying R_s does not improve the overall agreement between experimental and approximate results. The source current waveform contains odd harmonics only and the first ten are used in the PSPICE calculation. Figure 3 shows the experimental waveforms for input voltage, input current and output voltage. Figure 4(a) shows the frequency spectrum generated by PSPICE for R_s=0.33 and Figure 4(b) shows the actual spectrum obtained from a power quality analyzer.

Examination of Table 1 shows that there is broadly very good agreement between the approximate analysis, PSPICE simulation and experimental results.

Table 1

Calculated and Experimental Results for the Full Wave Bridge Rectifier					
	R_s=0		R_s=0.33		
	Calculated	**PSPICE**	**Calculated**	**PSPICE**	**Experimental**
Average Output Voltage V_0(V)	23.5	22.8	22.6	21.3	22.2
Average Output Current I_0(A)	1.07	1.0	1.0	1.0	1.0
Voltage Ripple ΔV(V)	1.07	0.91	1.07	0.73	1.2
Peak Diode Current Ip(A)	23.0	19.7	7.2	5.7	6.1
Power Factor k_p	0.37		0.67		0.63
THD%	251	214	112	118	121

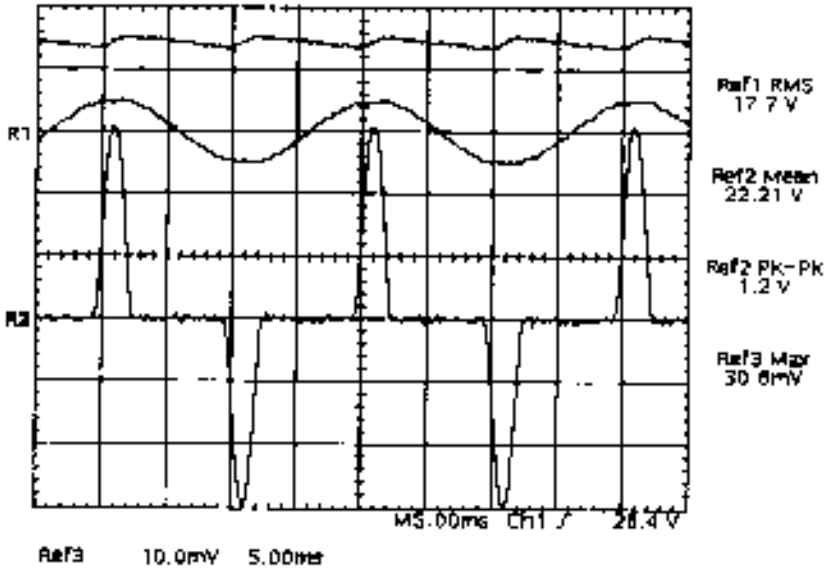

Figure 3: Experimental Waveforms: R1 Input Voltage 50V/div, R2 Output Voltage 5V/div, R3 Output Current 2A (10mV)/div, 5ms/div

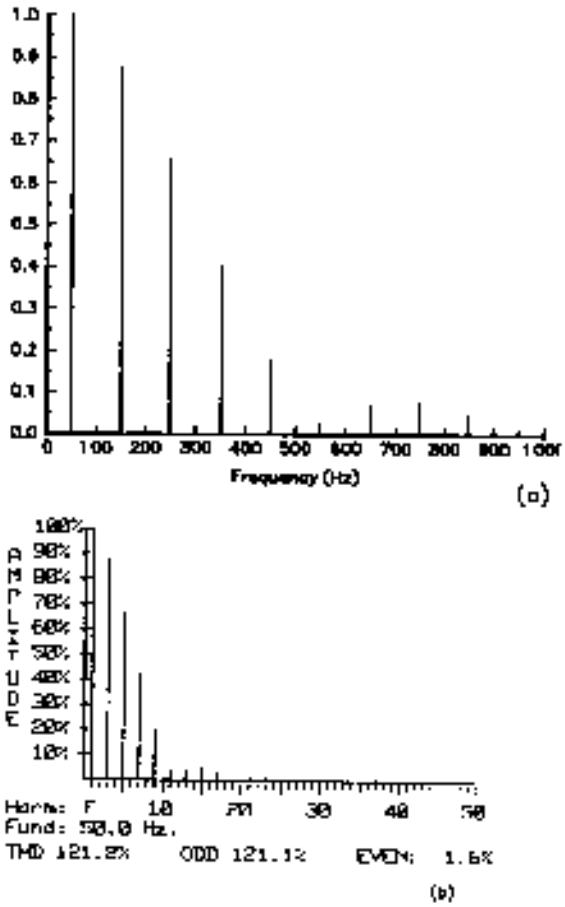

Figure 4: Fourier Analysis (a) PSPICE, (b) Experimental

Three Phase Operation

A three-phase supply is shown in Figure 5(a), which is connected to a three-phase load consisting of three full-wave rectifiers connected in star. This could be a large office complex with many personal computers and printers which have rectifier inputs. This is a three-phase balanced non-linear load. The neutral current is zero in a balanced three-phase linear load.

The load current is 100 A. Consider the case where the output voltage ripple ($\Delta V/V_s$) is 10%, the power factor found with (13) is 0.42. The R.M.S. value of the phase current is

$$I_a = \frac{\langle p \rangle}{k_p V_s} = \frac{\sqrt{2} V_s I_o}{k_p V_s} = \frac{\sqrt{2}\,100}{0.42} = 332 \text{ A}$$

The phase currents appear in pulses as shown in Figure 5(b).

The neutral current is the sum of the phase currents. The R.M.S. value of the current in the neutral is

$$I_n = \sqrt{I_a^2 + I_b^2 + I_c^2} = \sqrt{3} I_a = \sqrt{3}\, 332 = 575\,A$$

In a balanced linear three-phase load, the phase currents add to zero in the neutral, here the neutral current is almost double the line or phase currents.

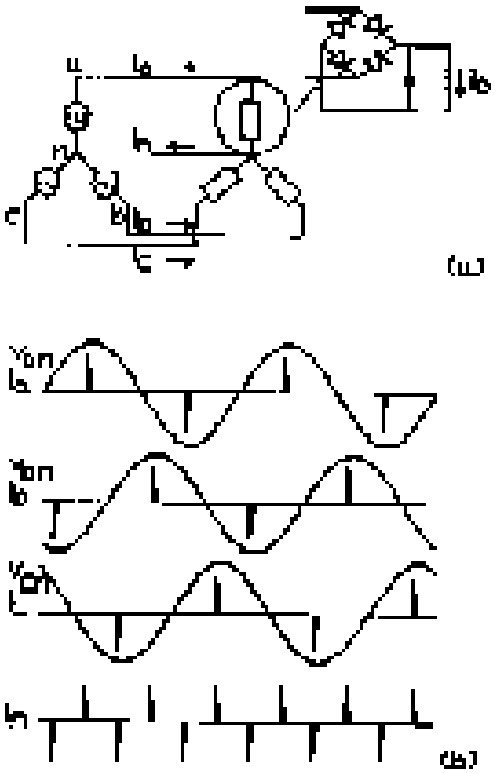

Figure 5: Three-Phase Non-Linear Load (a) Circuit, (b) Voltage and Current Waveforms

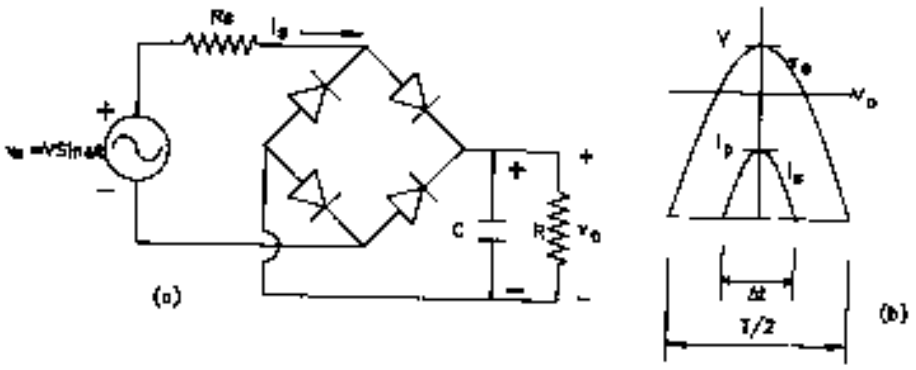

Figure A1: Full Wave Rectifier with Source Resistance R (a) Circuit Diagram,(b) Voltage and Current Waveforms

Conclusions

A general theory of power factor has been presented. The definition of power factor ties together concepts such as distortion factor, displacement factor and total harmonic distortion, in a consistent manner. It has been shown that knowledge of the fundamental harmonic of a complex waveform is sufficient in many cases of practical interest.

Simple, but effective, approximations have been derived for a circuit, which is very difficult to analyze. The general concept of power quality is explained in terms of a circuit, which is familiar to students and is, in itself, an example of poor power quality. Experimental results have been presented and the theories have been verified.

References

[1] Ridler, P.F., Rhod, F. 'Analysis of Single-Phase Capacitor-Input Rectifier Circuits', Proc. IEE, Vol. 117, No. 12, December 1970.

[2] Schade O.H. 'Analysis of Rectifier Operation', Proc. Inst. Radio Engrs., Vol. 31, 1943.

[3] Gray, P.E., Cambell, L.S. 'Electronic Principles: Physics, Models and Circuits', Wiley, New York, 1969.

Appendix A: Including a Source Resistance R_s

The source resistance R_s, shown in Figure A1 (a), slows down the charging rate of the capacitor. As the load current increases, the average load voltage decreases allowing the diode conduction interval to increase. Additional charge is placed on the capacitor to supply the increased load current. Charge balance must be maintained and therefore (9) still applies. The shape of the charging current becomes more sinusoidal, as shown in Figure A1 (b). The analysis which follows is based on that developed by Grey and Searle [3]. It assumes that R_S includes all parasitic effects; diode voltage drop, source resistance, etc.

In this analysis, the origin is taken at the peak of the input voltage and the diode conduction interval is $\pm\frac{\Delta t}{2}$. The supply current is

$$i_s(t) = \frac{\mathbf{V}\cos\omega t - V_o}{R_s} \qquad \text{(A1)}$$

Performing the integration in (9), and noting that the peak supply current is

$$I_p = \frac{\mathbf{V} - V_o}{R_s}$$

gives

$$\frac{\mathbf{V}}{R_s}\left[1 - \frac{V_o}{\mathbf{V}}\right]\frac{\Delta t}{T} = I_o \qquad \text{(A2)}$$

At $\omega t = \omega$ t/2 the supply voltage is equal to the load voltage and the diode conduction ceases

$$V_o = \mathbf{V}\cos(\omega\frac{\Delta t}{2}) \approx \mathbf{V}\left[1 - \frac{1}{2}\left(\frac{\omega\Delta t}{2}\right)^2\right]$$

Rearranging

$$1-\frac{V_o}{\mathbf{V}}=\frac{\pi^2}{2}\left(\frac{\Delta t}{T}\right)^2 \qquad \text{(A3)}$$

Combining (A2) and (A3) yields

$$\frac{\mathbf{V}_o}{V}=1-\frac{1}{\sqrt[3]{2}}\left[\frac{\pi R_s I_o}{\mathbf{V}}\right]^{\frac{2}{3}} \qquad \text{(A4)}$$

The peak value of the supply current is

$$I_p=\frac{\mathbf{V}-V_o}{R_s}=\left[\frac{\mathbf{V}}{2R_s}\right]^{\frac{1}{3}}(\pi I_o)^{\frac{2}{3}} \qquad \text{(A5)}$$

and

$$\frac{\Delta t}{T}=\sqrt[3]{\frac{2R_s I_o}{\pi^2\mathbf{V}}} \qquad \text{(A6)}$$

The displacement factor is unity. Performing the integration outlined in Section II, the distortion factor of the source current in (A1) is

$$k_d=\frac{\frac{D}{\sqrt{2}}-\frac{1}{\sqrt{2}\pi}\sin\pi D}{\sqrt{D+\frac{D}{2}\cos\pi D-\frac{3}{2\pi}\sin\pi D}} \qquad \text{(A7)}$$

where

$$D=\frac{\Delta t}{\frac{T}{2}} \qquad \text{(A8)}$$

This expression is not amenable to simplification. An alternative approach is to represent each current pulse with a sinewave of half-period DT/2, giving

$$k_d=\frac{4\sqrt{D}}{\pi}\frac{\cos\frac{\pi D}{2}}{1-D^2}\approx\frac{4\sqrt{D}}{\pi}$$

and taking D in (A8) using (A6)

$$k_p = 1.38 \sqrt[6]{\frac{R_s I_o}{\mathbf{V}}} = 1.3 \sqrt[6]{\frac{R_s I_o}{V_s}} \qquad \text{(A9)}$$

This is a simple straightforward equation for the power factor, which solves an extremely complex analytical problem. On first examination, it would appear from (A9) that the power factor is zero for R_s=0. It must be recalled that these are simple approximations of a very complex circuit and as the experimental results have shown they are extremely effective in calculating parameters of interest. In the example given, the value of peak diode current given by (A5) for R_s=0.01 corresponds to that given by (12) for R_s=0, so clearly in cases of practical interest the formulas work very well.

Biographical Summary

William Gerard Hurley (M'77, SM'90) was born in Cork, Ireland. He graduated from the National University of Ireland, Cork in 1974 with a Bachelor's degree (hons) in electrical engineering. He completed the Master's degree in electrical engineering at the Massachusetts Institute of Technology in 1976. He completed the Ph.D. on Transformer Modeling at the National University of Ireland, Galway in 1988.

He worked for Honeywell Controls in Canada as a product engineer from 1977 to 1979 and as a Development Engineer in transmission lines at Ontario Hydro from 1979 to 1983. He lectured in electronic engineering at the University of Limerick, Ireland from 1983 to 1991 and is currently Associate Professor of electrical engineering in the Department of Electronic Engineering at the National University of Ireland, Galway. He is the Director of the Power Electronics Research Center there. He was visiting professor of electrical engineering at the Massachusetts Institute of Technology in 1997/1998. Research interests include high frequency magnetics and power quality.

Prof. Hurley is a member of the Administrative Committee of the Power Electronics Society of the IEEE and a member of Sigma Xi. He is General Chair for the IEEE Power Electronics Specialists Conference in 2000.

A STUDY ON THE HARMONIC ANALYSIS AND FILTER DESIGN ON DISTRIBUTION SYSTEM USING SUPERHARM

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Introduction

The increasing application of power electronic equipment [especially (ASDs: adjustable-speed drives)] on distribution systems has led to a growing concern for harmonic distortion and the resulting impacts on system equipment and operations. The ASDs drives a process, whether fluid, gas, material, or air with a variable speed induction motor. Modern ASDs employ power electronic devices to generate the variable frequency power supply for AC motor speed control. Assessment and mitigation of the ASD harmonic effects on supply systems have become an important aspect of power quality management [1].

Harmonic simulations are used to quantify the distortion in voltage waveforms in a power system. Computer simulation is one of the effective ways to assess the harmonic effects of ASDs.

The utility has the responsibility of supplying to the customer a certain degree of quality power and the customer has the responsibility of not disrupting this quality of power in a manner that would affect other customers or the utility itself. Standards exist that serve as guidelines for the limits of power quality for the utility and the customer, such as IEEE 519-1992.

The aim of this study is to calculate the quantity of harmonic voltage by varying the ASD side load and to design the optimal harmonic filter for the elimination of harmonics.

Basic Definition and Concepts Related Harmonics

Distortion Indices

The most commonly used measure of deviation of a periodic waveform from a sinewave is called total harmonic distortion (THD) or distortion factor.

$$\mathrm{THD} = \frac{1}{M_1}\sqrt{\sum_{h=2}^{\infty} M_h^2} \qquad (1)$$

where M_h is the rms value of harmonic component h of the quantity M. THD is the measure of the effective value of the harmonic components of a distorted waveform, that is, the potential heating value of the harmonics relative to the fundamental [2].

Frequency Scan

Frequency scan is the simplest and most commonly used technique for harmonic analysis. It calculates the frequency response of a network seen at a particular bus or node. It refers to a plot showing the magnitude and phase of the driving point impedance (of the linear network) at a bus of interest versus frequency. Typically a 1 per unit sinusoidal current (or voltage) is injected into the bus of interest and the voltage (or current) response is calculated [5].

Frequency scan analysis is the most effective tool to detect harmonic resonance conditions in a system. This allows for locating resonant frequencies and determining if the network is in resonance at a particular harmonic. It has also been widely used for filter design.

Point of Common Coupling

IEEE 519 defines the point of common coupling (PCC) as:

"A point of metering or any point as long as both utility and the customer can either access the point for direct measurement of the harmonic indices meaningful to both or estimate the harmonic indices at a point of Interference through mutually agreeable methods."

This is the location where limits are applied. Generally, it will be at the high side of the customer step-down transformer.

System Model

A 69 kV radial distribution system as shown in Figure 1 was analyzed in the frequency domain, using SuperHarm®. The simulation results were analyzed using TOP®, The Output Processor. The ASD side load was varied and the effect of the variation was observed.

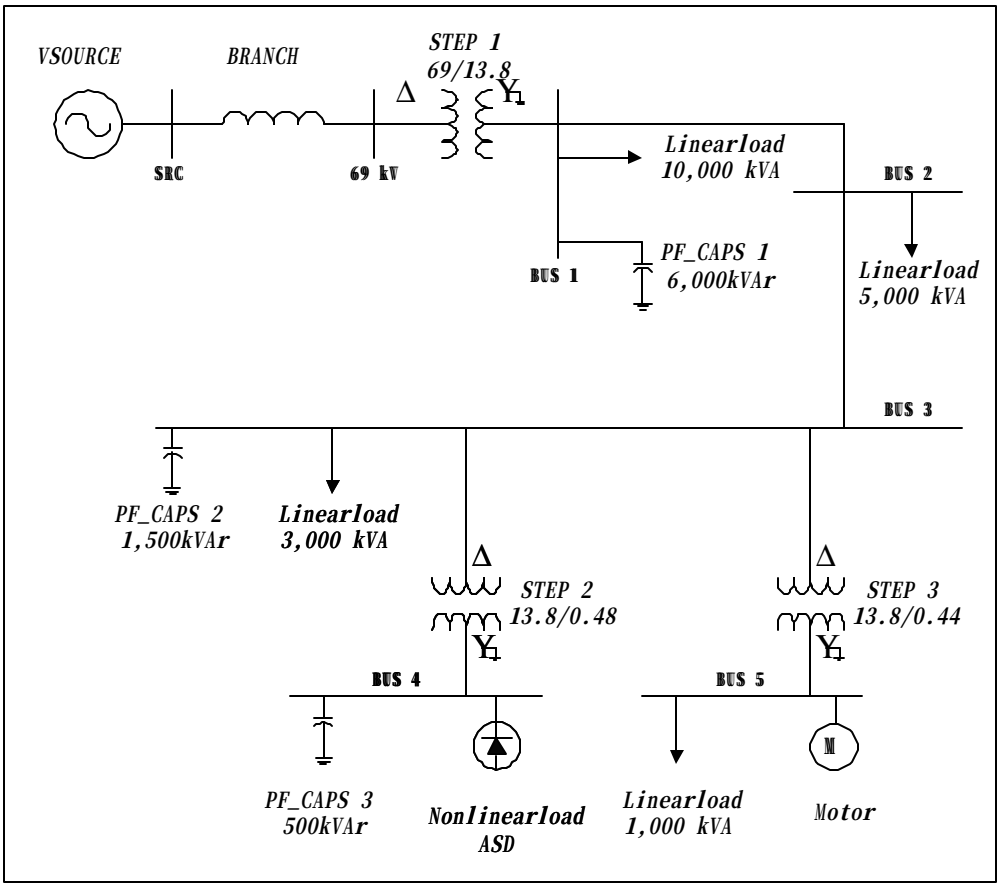

Figure 1: 69 kV Radial Distribution System Used for Simulations

Simulation Results

Varying the ASD Side Load

This simulation aims to observe that variation of harmonics at the buses as the ASD side load is varied. Table 1 summarizes the different situations related to the varying the ASD side load.

Table 1: Cases studies

CASE	Varying the ASD side load
Case 1	100 % Load
Case 2	75 % Load
Case 3	50 % Load

Case 1: 100% Load

Case 1 represents harmonic voltage distortion at the buses under 100 % load condition. Because ASD is a significant source of harmonics, it injects harmonic currents into the distribution system. Therefore, voltage distortion is the result of distorted currents passing through the linear, series

impedance of distribution system. Table 2 shows harmonic summary data relating to the voltage distortion at the buses. Also, The harmonic spectrum given in Figure 2 shows voltage distortion at the buses.

Table 2: Harmonic Summary Data (100 % Load)

Name	Fund	% THD	H3	H5	H7	H9	H11	H13
69kV_A	39068.0	3.79771	9.38E-12	1446.76	317.717	1.25E-11	40.3645	75.0134
Bus1_A	7694.59	7.72819	6.50E-12	579.854	127.335	2.29E-11	16.1769	30.0628
Bus2_A	7680.53	7.69889	6.68E-12	578.216	121.142	2.03E-11	13.1617	21.6978
Bus3_A	7678.12	7.69919	6.72E-12	578.337	120.089	1.99E-11	12.6171	20.1776
Bus4_A	266.708	8.99391	0.048544	16.1394	9.22254	0.407921	5.12611	14.1960
Bus5_A	242.717	7.56560	3.19E-13	17.9652	3.72916	1.05E-12	0.39165	0.62626

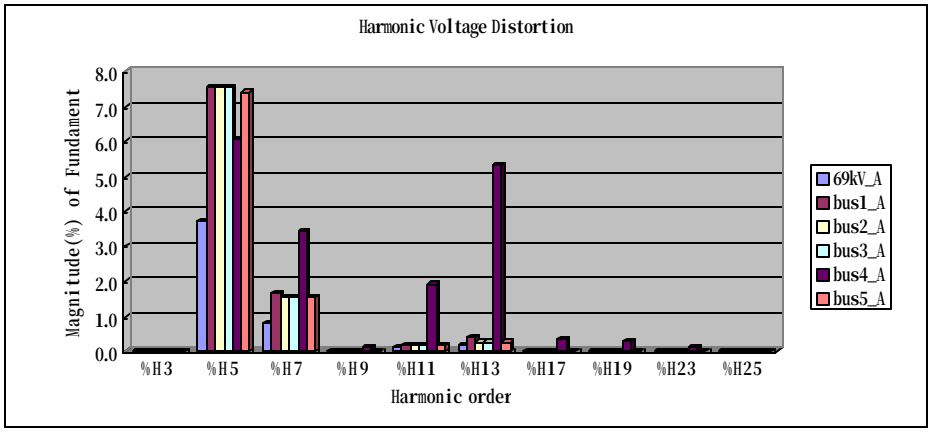

Figure 2: Harmonic voltage at the Buses due to the ASD at the Bus4 (100 % Load)

Case 2: 75% Load

Case 2 represents harmonic voltage distortion at the buses under 75 % load condition.
Table 3 shows harmonic summary data relating to the voltage distortion at the buses. Also, The harmonic spectrum given in Figure 3 shows voltage distortion at the buses.

Table 3: Harmonic Summary Data (75 % Load)

Name	Fund	% THD	H3	H5	H7	H9	H11	H13
69kV_A	39057.4	4.39808	1.58E-11	1656.53	446.389	7.97E-12	71.9941	43.7362
bus1_A	7690.19	8.95261	1.10E-11	663.928	178.905	1.46E-11	28.8531	17.5280
bus2_A	7675.96	8.91236	1.13E-11	662.053	170.204	1.30E-11	23.4752	12.6508
bus3_A	7673.53	8.91149	1.13E-11	662.192	168.724	1.27E-11	22.5038	11.7645
bus4_A	266.281	9.91848	0.081701	18.4795	12.9576	0.260652	9.14294	8.27691
bus5_A	242.572	8.75681	5.38E-13	20.5700	5.23943	6.74E-13	0.698557	0.365137

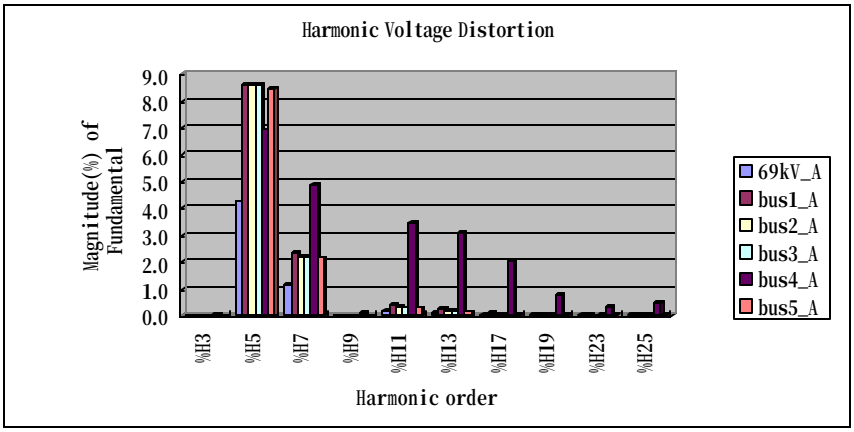

Figure 3. Harmonic Voltage at the Buses due to the ASD at the Bus4 (75 % Load)

Case 3: 50% Load

Case 3 represents harmonic voltage distortion at the buses under 50 % load condition.
Table 4 shows Harmonic summary data relating to the voltage distortion at the buses. Also, The harmonic spectrum given in Figure 4 shows voltage distortion at the buses.

Table 4: Harmonic Summary Data (50 % Load)

Name	Fund	% THD	H3	H5	H7	H9	H11	H13
69kV_A	39068.0	4.77817	1.45E-11	1786.21	519.165	5.99E-12	153.995	18.8987
bus1_A	7694.59	9.72337	1.00E-11	715.903	208.073	1.10E-11	61.7164	7.57396
Bus2_A	7680.53	9.66797	1.03E-11	713.881	197.953	9.77E-12	50.2132	5.46649
Bus3_A	7678.12	9.66503	1.04E-11	714.031	196.232	9.55E-12	48.1354	5.08351
Bus4_A	266.708	12.3546	0.074897	19.9261	15.0701	0.195802	19.5567	3.57651
Bus5_A	242.717	9.49723	4.93E-13	22.1803	6.09364	5.06E-13	1.49421	0.15778

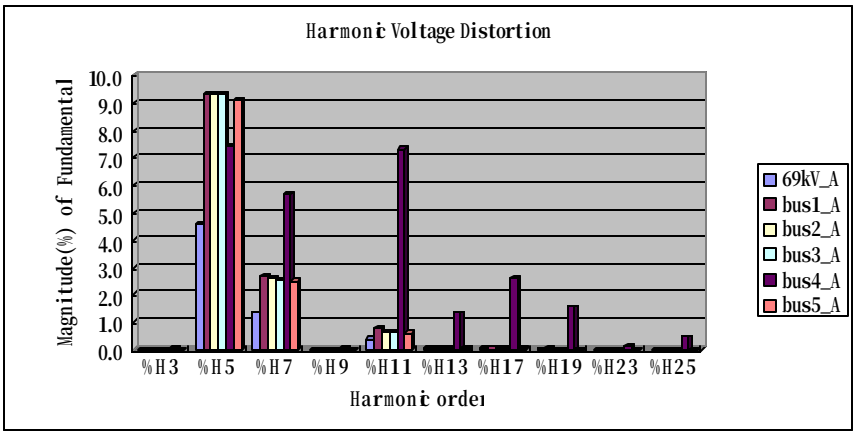

Figure 4: Harmonic Voltage at the Buses due to the ASD at the Bus4 (50 % Load)

In the distribution system as shown in Figure 1, bus1 is considered as PCC. Case 1 to 3 shows that the harmonic voltage distortion does not remain within IEEE Standard 519 limits of 5 percent THD at PCC. To remain within IEEE Standard 519 limits, a harmonic filter is needed.

Filter Design

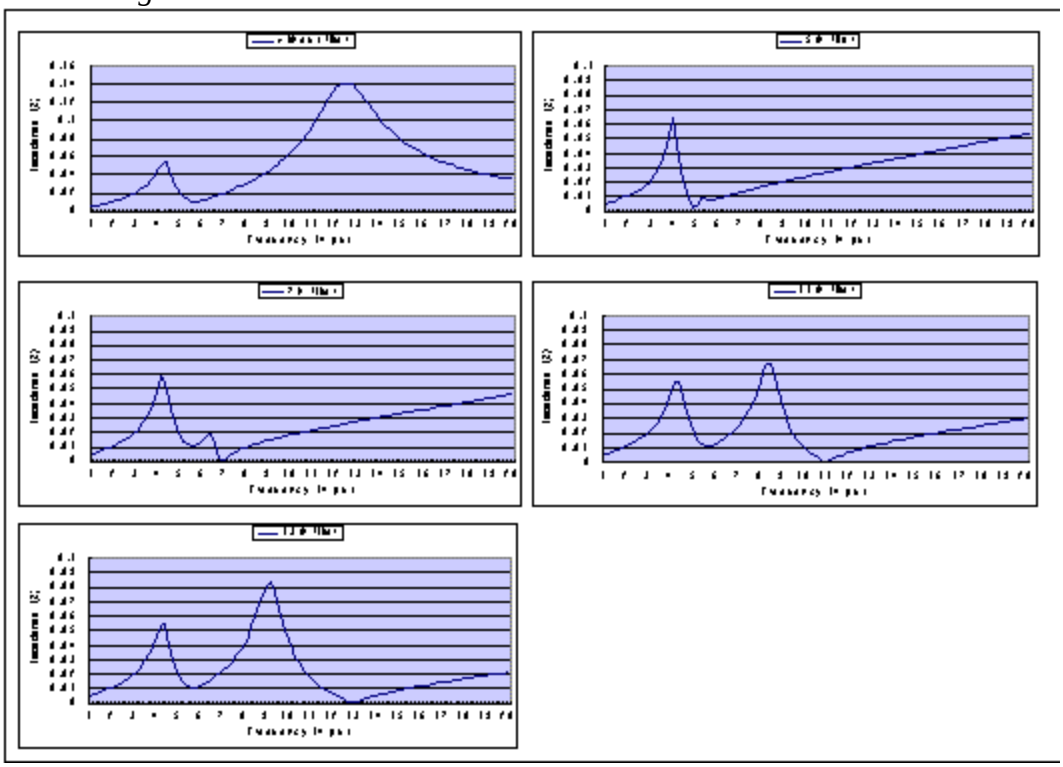

Figure 5: Frequency Scan at the Bus 1_A

Figure 5 shows frequency scan at the bus 1_A. It shows that the difference in the case where each filter is installed and not installed.

Filters are the most common solution because a filter can provide reactive power support at the fundamental frequency and a low impedance path for one or more harmonic current components to flow.

Each harmonic filter (5^{th}, 7^{th}, 11^{th}, 13^{th}) that was replaced with PF_CAP3 added to bus4. Previously, this simulation was carried out with 100% load condition. The harmonic spectrum given in Figure 6 to 8 shows voltage distortion at the buses. It shows the difference in case where the filter is installed and not.

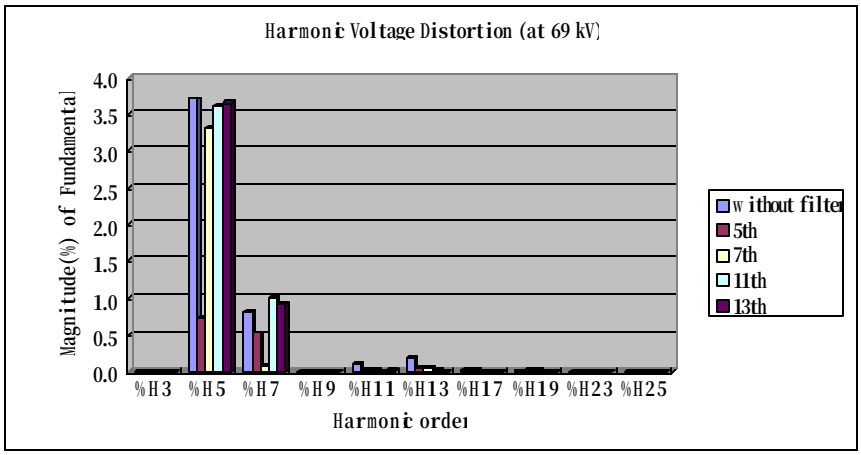

Figure 6: Comparison without Harmonic Filter and the with each Harmonic Filter at the 69 kV_A bus (100 % Load)

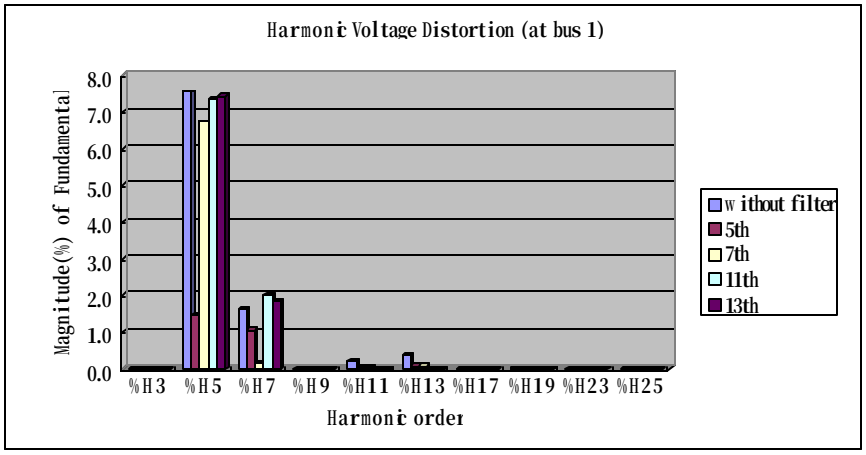

Figure 7: Comparison without Harmonic Filter and the with each Harmonic Filter at the Bus 1_A Bus (100 % Load)

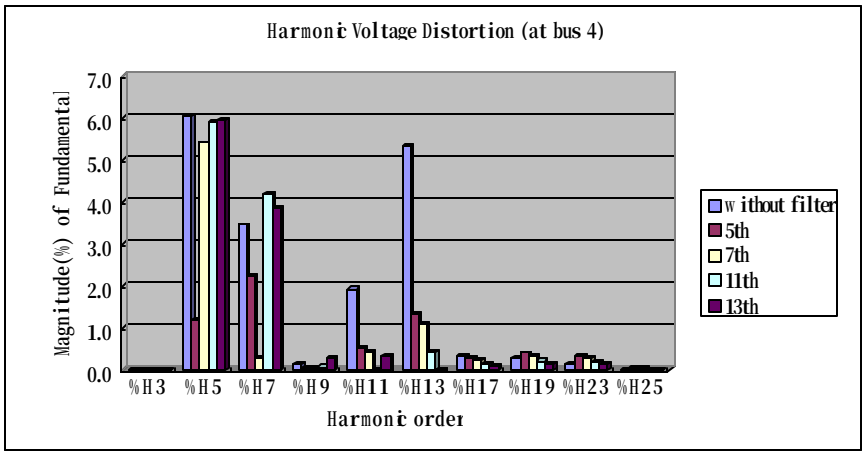

Figure 8: Comparison without Harmonic Filter and the with each Harmonic Filter at the Bus 4_A Bus (100 % Load)

Figure 6 to 8 show that 5th filter is optimal. After installing the 5th filter, harmonic problems on the distribution system reduce. This is the same with 100% load condition. The 5th filter is proper under other load conditions (75 %, 50 %).

When the 5th filter is installed, the harmonic spectrum given in Figure 9 to 11 shows voltage distortion at the buses.

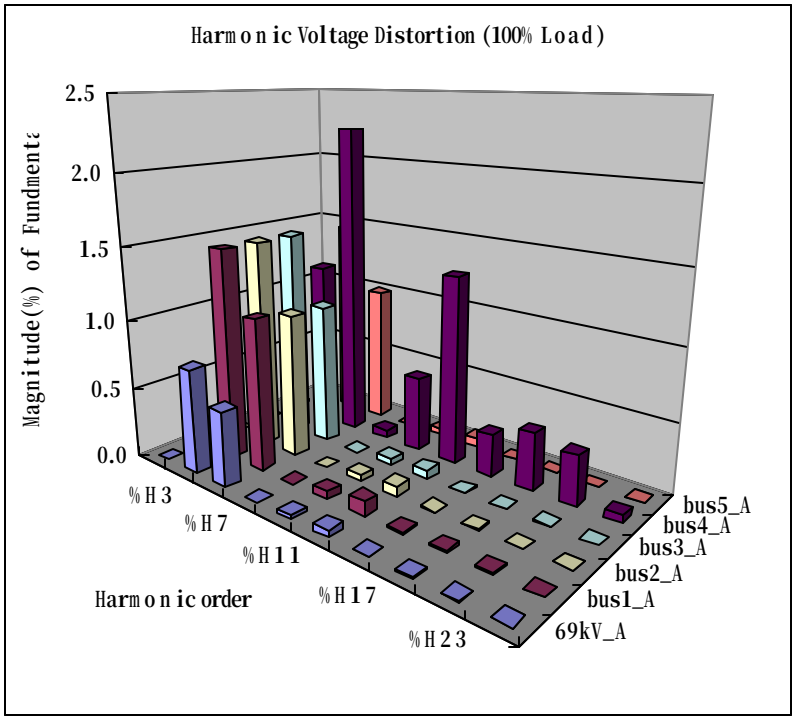

Figure 9: Harmonic Voltage at the Buses when 5th Filter Installs (100 % Load)

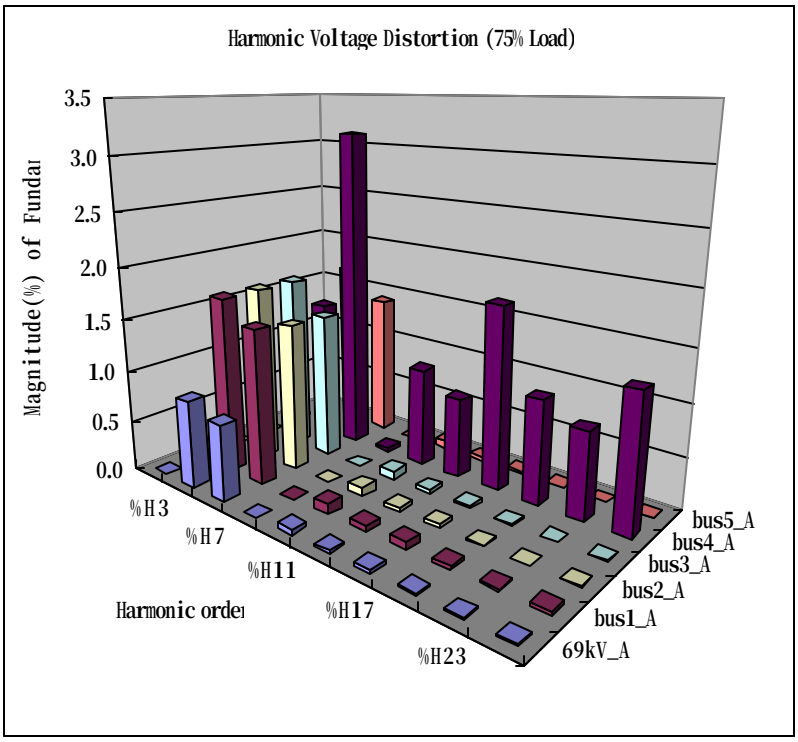

Figure 10: Harmonic Voltage at the Buses when 5th Filter Installs (75 % Load)

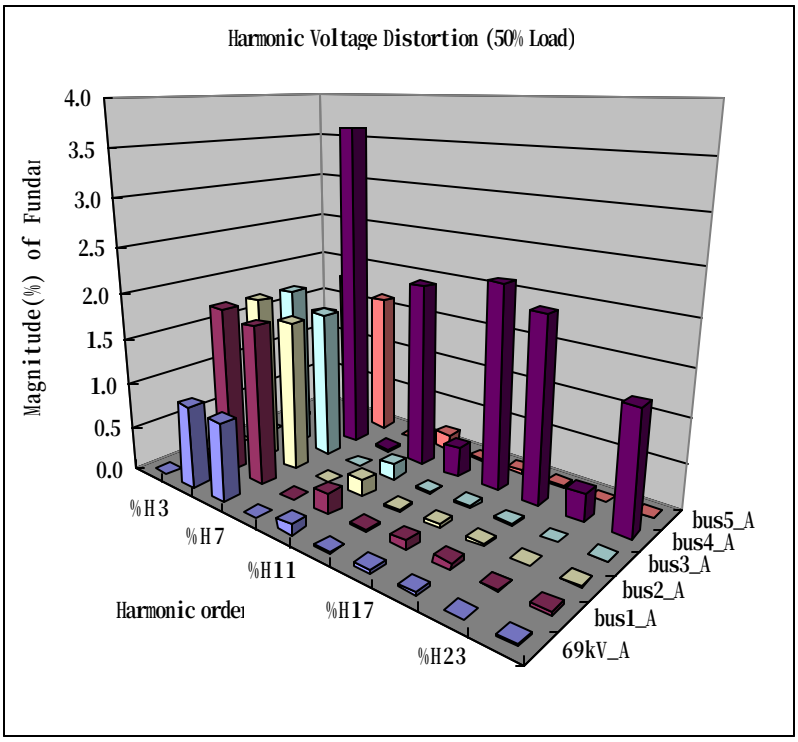

Figure 11: Harmonic Voltage at the Buses when 5th Filter Installs (50 % Load)

Conclusions

1. As the ASD side load decreased, the total harmonic distortion at the buses increased.
2. The total harmonic distortion varies as the ASD side load is varied. But the harmonic voltage distortion does not remain within IEEE Standard 519 limits of 5 percent THD at PCC. To remain within IEEE Standard 519 limits, a harmonic filter is needed.
3. When the 5th filter is installed, the harmonic voltage distortion remains within the IEEE Standard 519 limits of 5 percent THD at the PCC.

References

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