PQSoft Case Study

Voltage Magnification and Nuisance Tripping during Capacitor Bank Switching

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Abstract:

The application of utility capacitor banks has long been accepted as a necessary step in the efficient design of utility power systems. In addition, capacitor switching is generally considered a normal operation for a utility system and the transients associated with these operations are generally not a problem for utility equipment. These low frequency transients, however, can cause problems for low voltage power electronic-based loads.

Adjustable-speed drives are susceptible to dc link overvoltage trips caused by utility capacitor switching. In general, an increase in input inductance (choke or isolation transformer) will reduce the possibility of nuisance tripping. However, if the customer has power factor correction capacitors on the same bus, it may be necessary to take additional remedial actions. This case study investigates the potential for voltage magnification and nuisance tripping during utility capacitor bank switching on a 24kV distribution system.

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RELATED STANDARDS

IEEE Std. 1036-1992

GLOSSARY AND ACRONYMS

ASD	Adjustable-Speed Drive
PWM	Pulse Width Modulation
MOV	Metal Oxide Varistor
TVSS	Transient Voltage Surge Suppressors

INTRODUCTION AND MODEL DEVELOPMENT

The potential for voltage magnification and nuisance tripping during utility capacitor bank switching was studied for the system shown in Figure 1. The accuracy of the system model was verified using three-phase and single-line-to-ground fault currents and other steady-state quantities, such as capacitor bank inrush and rated current and voltage rise.

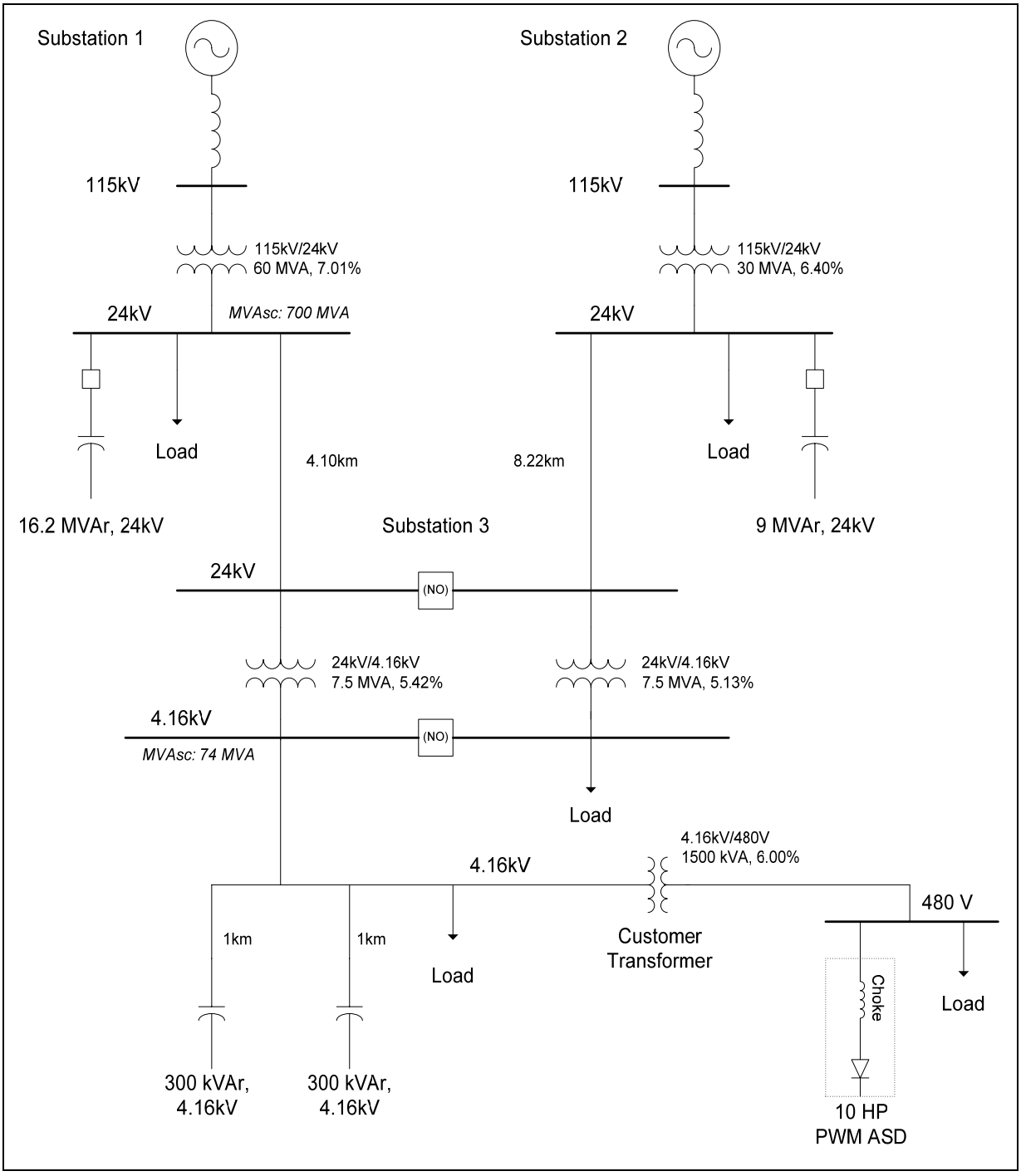

Figure 1 - Oneline Diagram for the Capacitor Bank Switching Case Study

Voltage magnification occurs when the transient oscillation initiated by the energization of a utility capacitor bank excites a series resonance formed by a step-down transformer and power factor correction capacitor bank on the utility's or customer's lower voltage system. The result is a higher overvoltage magnitude at the lower voltage bus. Previous research has indicated that the worst magnified transient occurs when the following conditions are met:

1. The rating of the switched capacitor bank is significantly larger (>10) than the lower voltage power factor correction bank (e.g., 16.2 MVAr vs. 300 kVAr).

2. The energizing frequency of the utility capacitor bank is close to the series resonant frequency formed by the step-down transformer and the lower voltage capacitor bank.

3. There is relatively little damping (resistive load) provided by the lower voltage load (typical industrial plant configuration - primarily motor load).

Nuisance tripping refers to the undesired shutdown of a customer's adjustable-speed drive or other power-electronic-based process device due to a transient overvoltage on the device's dc bus. Very often, this overvoltage is caused by utility transmission or distribution capacitor bank energization. Considering the fact that many distribution banks are time clock controlled, it is easy to see how this event can occur on a regular basis, thereby causing numerous process interruptions for the customer.

The nuisance tripping event consists of an overvoltage trip due to a dc bus overvoltage on voltage-source inverter drives. Typically, for the protection of the dc capacitor and inverter components, the dc bus voltage is monitored and the drive tripped when it exceeds a preset level. This level is typically around 780 volts (for 480 volt applications), which is only 120% of the nominal dc voltage. It is important to note that nuisance tripping can occur even if the customer does not have power factor correction capacitor banks.

An adjustable-speed drive system consists of three basic components and a control system as illustrated in Figure 2. The rectifier converts the three-phase ac input to a dc voltage, and an inverter circuit utilizes the dc signal to produce a variable magnitude, variable frequency ac voltage, that is used to control the speed of an ac motor.

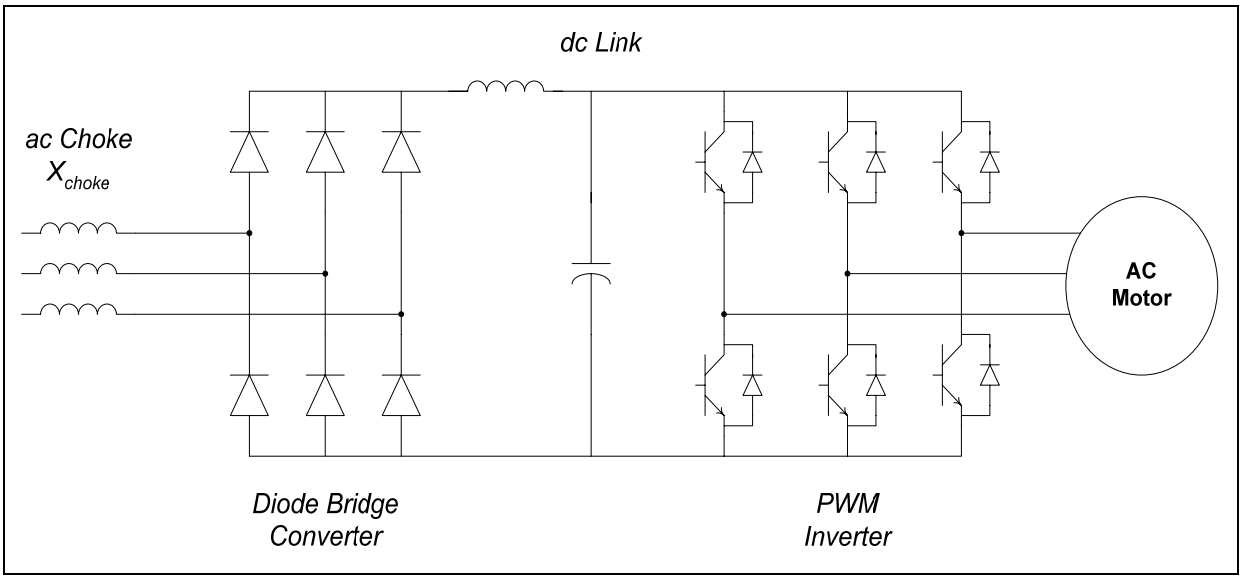

Figure 2 - Adjustable-speed Drive Simulation Model

SIMULATION RESULTS

Energizing a shunt capacitor bank from a predominantly inductive source creates an oscillatory transient that can approach twice the normal system peak voltage (V_{pk}). The characteristic frequency (f_s) of this transient is given by the following expression:

$$f_s = \frac{1}{2\pi\sqrt{(L_s * C)}} \approx f_{system} * \sqrt{\frac{X_c}{X_s}} = f_{system} * \sqrt{\frac{MVA_{sc}}{MVAr_{3\phi}}} = f_{system} * \sqrt{\frac{1}{\Delta V}}$$

where:

f_s = characteristic frequency (Hz)

L_s = positive sequence source inductance (H)

C = capacitance of bank (F)

f_{system} = system frequency (50 or 60 Hz)

X_s = positive sequence source impedance (Ω)

X_c = capacitive reactance of bank (Ω)

MVA_{sc} = three-phase short circuit capacity (MVA)

$MVAr_{3\varphi}$ = three-phase capacitor bank rating (MVAr)

ΔV = steady-state voltage rise (per-unit)

The energizing frequency for the 16.2 MVAr, 24kV (74.60μF) distribution capacitor bank with a source strength ($I_{3\varphi}$) of 16.85 kA (2.18mH) may be approximated using the following expression:

$$f_s \approx f_{system} * \sqrt{\left(\frac{MVA_{sc}}{MVAr_{3\phi}}\right)} = 60 * \sqrt{\left(\frac{700.44}{16.2}\right)} = 394.5\,Hz$$

where:

$$MVA_{sc} = \sqrt{3} * 24kV * 16.85kA = 700.44\,MVA$$

The steady-state voltage rise for this case may be approximated using the following expression:

$$\Delta V = \left(\frac{MVAr_{3\phi}}{MVA_{sc}}\right) * 100 = \left(\frac{16.2}{700.44}\right) * 100 = 2.3\%$$

Finally, the peak inrush current (I_{pk}) (refer to Figure 3) may be approximated using the following expression:

$$I_{pk} = \frac{V_{pk}}{\sqrt{\left(\frac{L_s}{C}\right)}} = \frac{24kV * \left(\sqrt{2}/\sqrt{3}\right)}{\sqrt{\left(\frac{2.18mH}{74.60\mu F}\right)}} = 3625A$$

where:

V_{pk} = peak system voltage (line-to-ground)

L_s = positive sequence source inductance (H)

C = capacitance of bank (F)

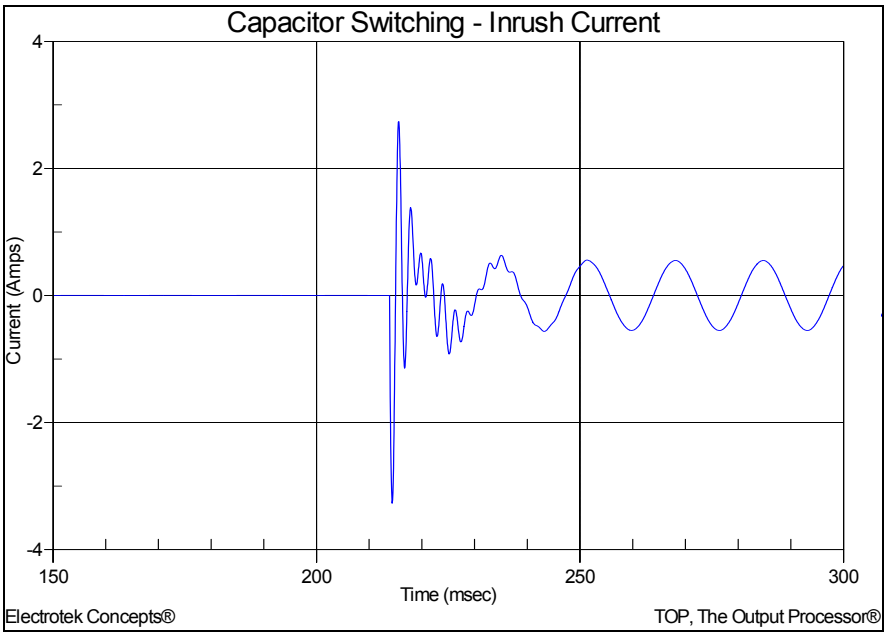

Figure 3 - Inrush Current during Capacitor Bank Energization

It is important to note that the peak inrush current is estimated without including resistance in the calculation, and in general, actual and simulated values are somewhat lower. The peak simulated inrush current for the 16.2 MVAr capacitor bank was 3273 amps (90% of calculated value).

The maximum transient overvoltage (refer to Figure 4) at the 24kV substation bus when energizing the 16.2 MVAr capacitor bank was 1.66 per-unit. Typical overvoltage magnitude levels range from 1.3 to 1.8 per-unit for larger substation capacitor banks. The maximum transient overvoltage (refer to Figure 5) at the 4.16kV bus was 1.34 per-unit so voltage magnification did not occur for this system.

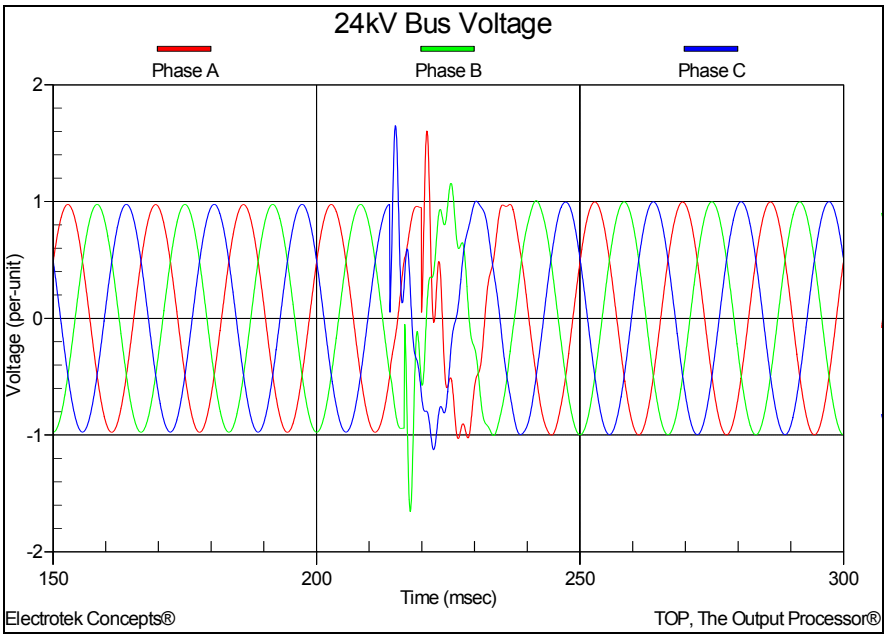

Figure 4 - Substation Bus Voltage during Capacitor Bank Energization

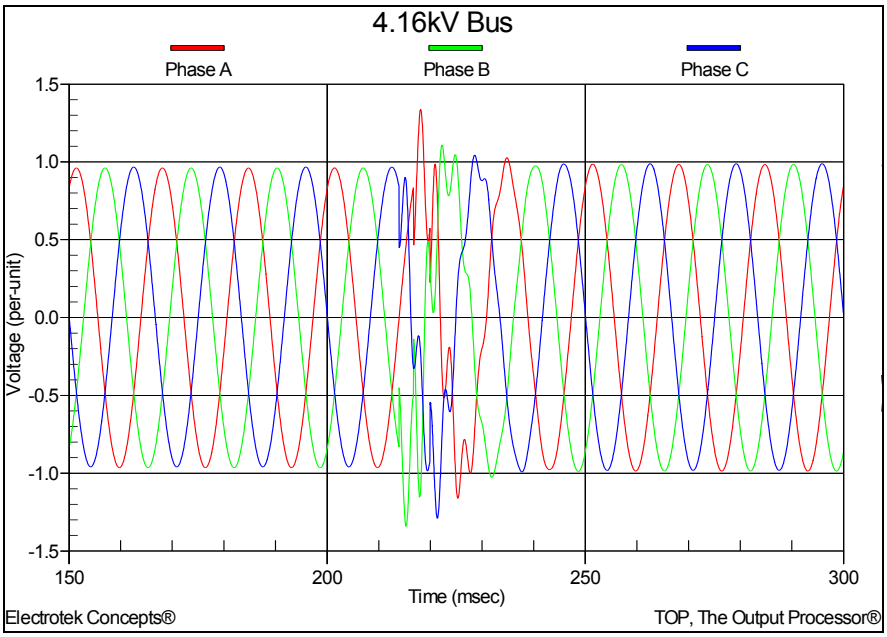

Figure 5 - 4.16kV Bus Voltage during Capacitor Bank Energization

Figure 6 shows the resulting dc voltage on the 10 hp adjustable-speed drive in the customer facility. The peak transient voltage is 808 volts, which is somewhat higher than the assumed trip level of 780 volts, so it is assumed that the drive will trip for this case.

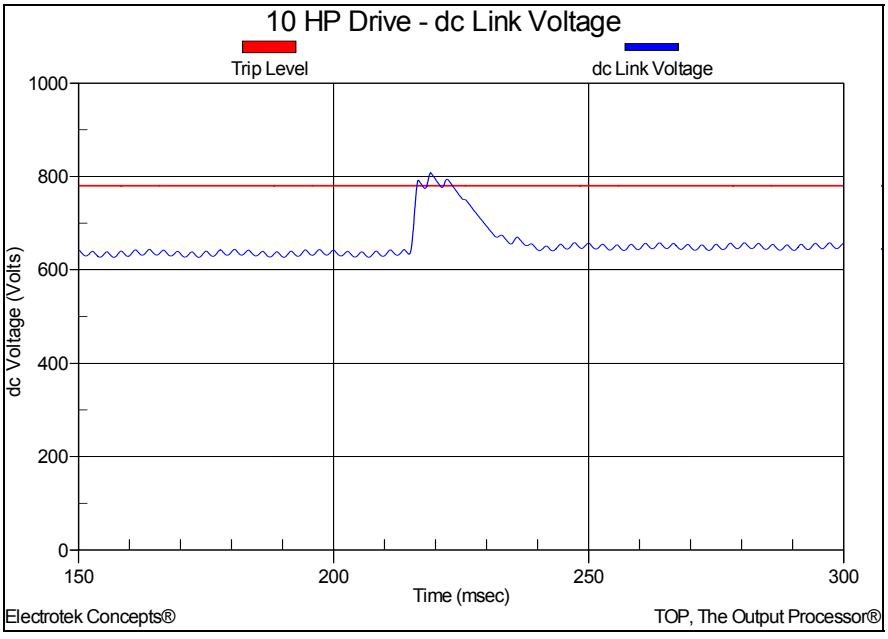

Figure 6 - ASD dc Link Voltage during Capacitor Bank Energization

The effectiveness of synchronous closing control on the substation capacitor bank switch was evaluated in a series of cases that varied the timing error from an ideal voltage zero closing. Synchronous closing is independent contact closing of each phase near a voltage zero. Previous analysis has indicated that a closing consistency of ±1.0msec provides overvoltage control comparable to properly rated pre-insertion resistors.

Figure 7 shows the resulting 24kV bus voltage for the worst-case synchronous closing control case with a +1.0msec error. The maximum transient overvoltage is reduced from 1.66 per-unit to 1.09 per-unit.

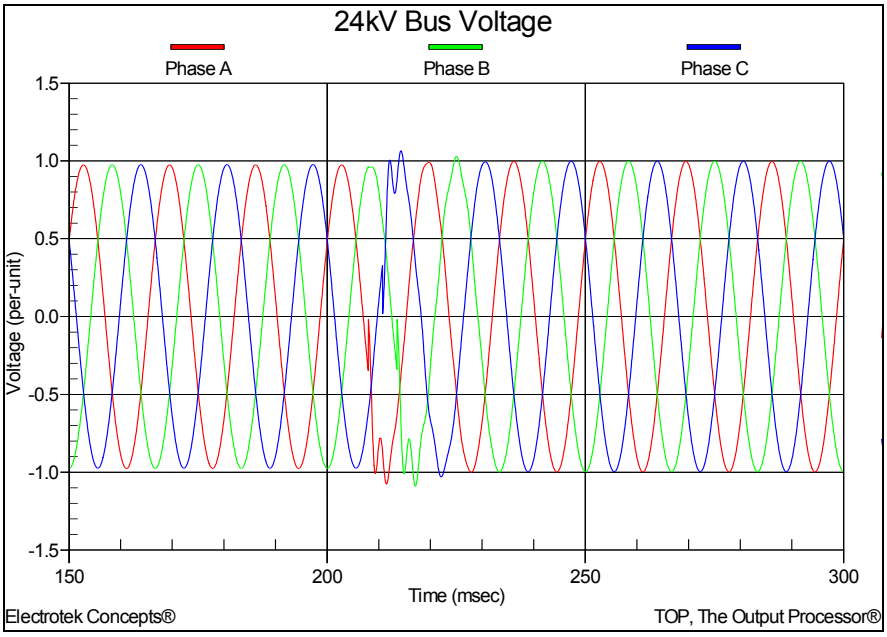

Figure 7 - Substation Bus Voltage with Synchronous Closing Control

Figure 8 shows the resulting dc link voltage for the adjustable-speed drive for the synchronous closing control case with a +1.0msec error. The dc overvoltage is reduced from 808 volts to 748 volts, so it is assumed that the drive will not trip for this case.

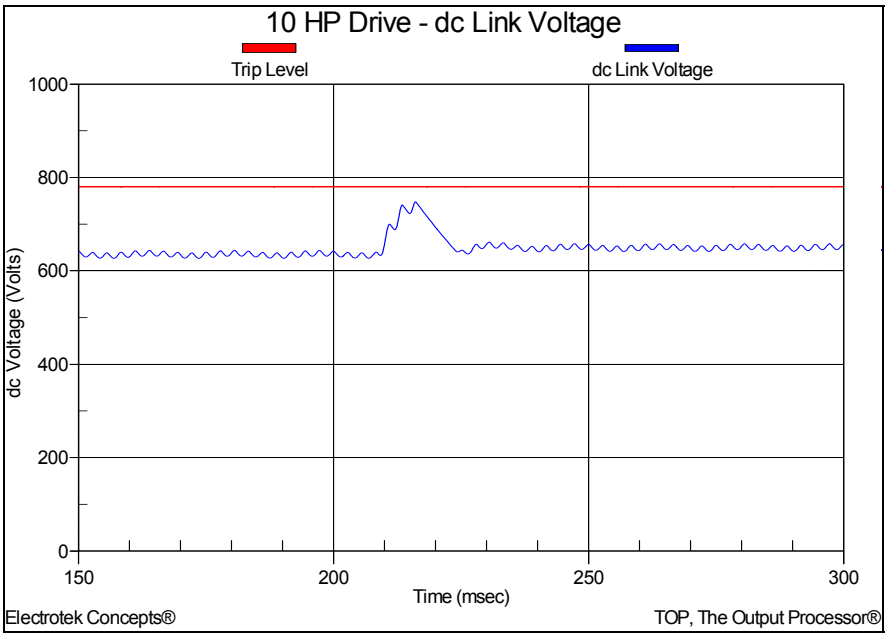

Figure 8 - ASD dc Link Voltage with Synchronous Closing Control

A pre-insertion resistance provides a means for reducing the transient currents and voltages associated with the energization of a shunt capacitor bank. The impedance is shorted-out (bypassed) shortly after the initial transient dissipates, thereby causing a second transient event. The insertion transient typically lasts for less than one cycle of the system frequency. The performance of pre-insertion impedance is evaluated using both the insertion and bypass transient magnitudes, as well as the capability to dissipate the energy associated with the event, and repeat the event on a regular basis.

Pre-insertion resistors and high-loss pre-insertion inductors are one of the most effective means for controlling capacitor bank energizing transients. The optimum resistor value for controlling capacitor bank energizing transients depends primarily on the capacitor bank rating and the source strength. It should be approximately equal to the surge impedance (Z_s) formed by the capacitor bank and source:

$$R_{optimum} \approx \sqrt{\left(L_s / C\right)}$$

where:

L_s = positive sequence source inductance (H)

C = capacitance of bank (F)

The optimum resistor rating for the 16.2 MVAr, 24kV (74.60μF) substation capacitor bank with a source strength ($I_{3\varphi}$) of 16.85 kA (2.18mH) may be approximated using the following expression:

$$R_{optimum} \approx \sqrt{\left(2.18\text{mH} / 74.60\mu\text{F}\right)} = 5.4\Omega$$

A 6.4Ω resistor was chosen for the simulation because it is available commercially. Figure 9 shows the resulting 24kV bus voltage for the 6.4Ω pre-insertion resistor case. The maximum transient overvoltage is reduced from 1.66 per-unit to 1.12 per-unit.

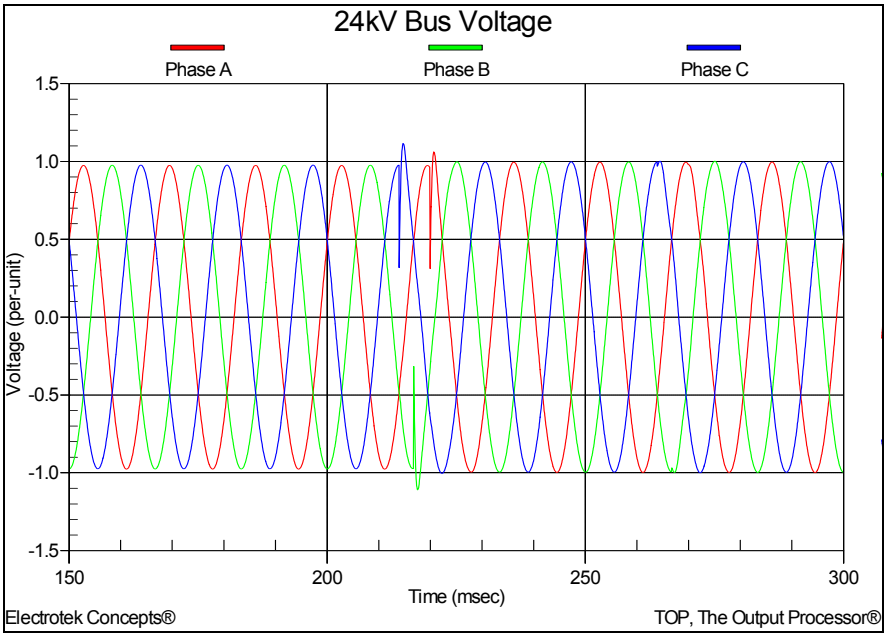

Figure 9 - Substation Bus Voltage with Pre-insertion Resistor

Figure 10 shows the resulting dc link voltage for the adjustable-speed drive for the 6.4Ω pre-insertion resistor case. The dc overvoltage is reduced from 808 volts to 710 volts, so it is assumed that the drive will not trip for this case.

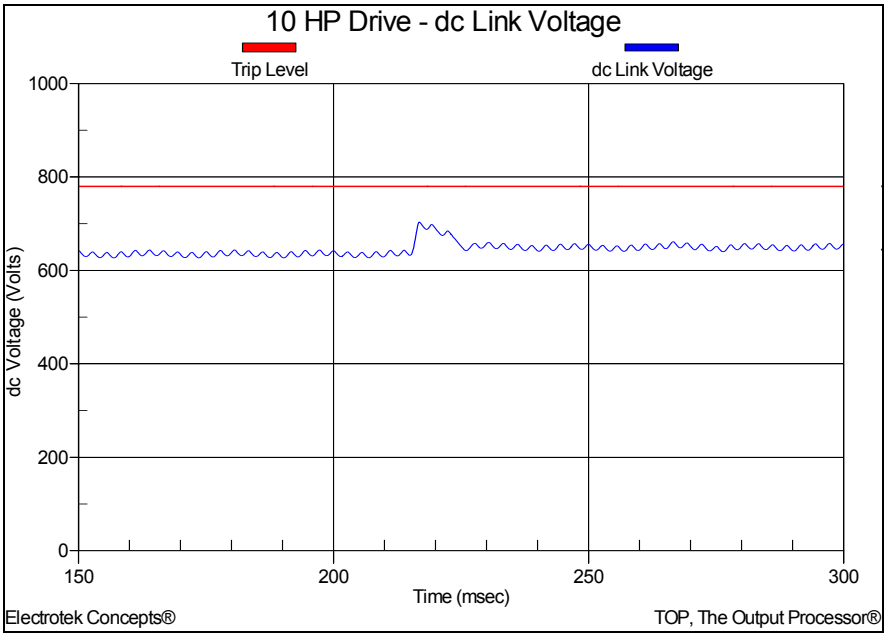

Figure 10 - ASD dc Link Voltage with Pre-insertion Resistor

The most effective methods for eliminating nuisance tripping are to reduce the energizing transient overvoltage, or to isolate the drives from the system with series inductors, often referred to as chokes. The additional series inductance of the choke will reduce the transient magnitude at the input to the drive and the associated current surge into the dc link filter capacitor, thereby limiting the dc overvoltage.

While determining the precise inductor rating for a particular application may require a detailed computer simulation study, a more common approach involves the widespread application of a standard 3% value. The 3% rating is based upon the drive kVA rating and is usually sufficient for most applications where voltage magnification is not also a concern. Generally, the choke is specified in *%X* and *hp*. However, the inductance of the choke may be approximated using the following relationship. A 3% choke for the customer's 10 hp drive would have the following inductance:

$$L_{choke} \approx \left(\frac{\left(\frac{kV_{\phi\phi}^2}{\left(hp / 1000 \right)} \right) * X\%}{2 * \pi * f_{system}} \right) = \left(\frac{\left(\frac{0.480^2}{\left(10 / 1000 \right)} \right) * 0.03}{2 * \pi * 60} \right) = 1.83mH$$

where:

f_{system} = system fundamental frequency (50 or 60 Hz)
X = inductive reactance of ac choke (%)
$kV_{\phi\phi}$ = system rms phase-to-phase voltage (kV)
hp = Horsepower rating of the drive (hp)

Figure 11 shows the resulting dc link voltage for the adjustable-speed drive with a 3% choke applied to the ac terminals. The dc overvoltage is reduced from 808 volts to 736 volts, so it is assumed that the drive will not trip for this case.

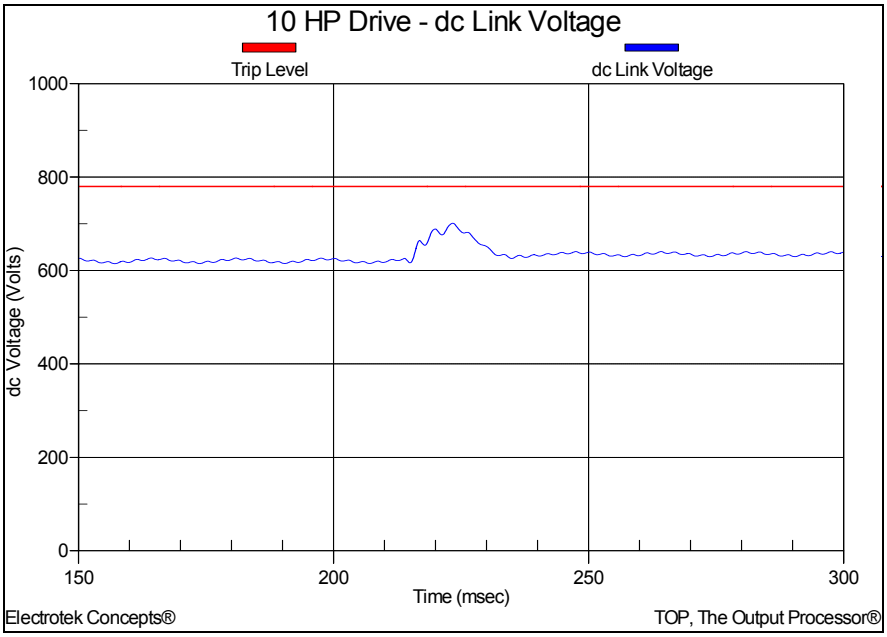

Figure 11 - ASD dc Link Voltage with a 3% Choke

SUMMARY

Observations and conclusions for this case study include:

1. The devices and equipment being applied on the power system are more sensitive to power quality variations than equipment applied in the past. New equipment includes microprocessor-based controls and power-electronic devices that are sensitive to many types of disturbances. Controls can be affected, resulting in nuisance tripping or misoperation as part of an important process, or actual device failure can occur.

2. Capacitor bank switch selection and configuration will generally depend on switch capabilities (e.g., short circuit interrupting and capacitance switching ratings), mitigation device selection (e.g., pre-insertion vs. synchronous closing), site considerations, and an economic evaluation.

3. Inrush currents during energization should be below rated breaker/switch capabilities.

4. Transient overvoltages related to voltage magnification at lower voltage buses were found to be below arrester protective levels for the simulated system. However, these transients may exceed levels that could cause nuisance tripping of adjustable-speed drives.

5. Transient overvoltages associated with energization of the 24kV capacitor bank can be significantly reduced with the application of synchronous closing control or pre-insertion resistors. In addition, the resulting overvoltages at distribution capacitor banks and lower voltage customer locations were also reduced, thereby significantly reducing the probability of localized customer problems due to sensitive equipment or low voltage power factor correction.

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